INSTITUTO TECNOLÓGICO DE COSTA RICA

ELECTRONICS ENGINEERING DEPARTMENT

Development of a low-frequency cell stimulator for regeneration/apoptosis experiments

A report submitted in partial fulfillment of the requirements for the Licentiate Degree in Electronics Engineering

Submitted by

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Cartago, Costa Rica

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INSTITUTO TECNOLÓGICO DE COSTA RICA

DEPARTMENT OF ELECTRONICS ENGINEERING

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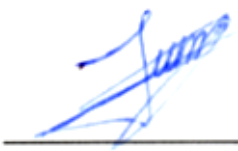

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Abstract

Cellular stimulation by exposition to variable frequency electric fields constitutes a method for modifying cellular characteristics such as metabolism, orientation, migration and biological function. For this type of study and behavior, high-cost and complex commercial equipment is often used, which shows in general low bandwidth that limits the scope of the experiments.

This work presents the design and implementation of a prototype for electric stimulation and impedance measurement of cell samples characterized by low-cost, portability, and easy reconfigurability of frequency and voltage, which makes it suitable for stimulation studies and research purposes. Also, it constitutes a preliminary study for systems with higher bandwidth, higher impedance range, and more input channels. The device is designed and implemented in order to carry out experiments of regeneration and apoptosis. It can generate electric signals up to 40 kHz at voltages in the range from 0 V to 100 mV, and it is capable of measuring impedance up to 1 MΩ. Experiments of cellular stimulation and impedance measurement were carried out over yeast cultures, and the results are compared with the ones obtained by the Agilent 4284A LCR meter.

Keywords: Cellular stimulation, impedance measurement, impedance spectroscopy, signal generation, ABBM.

Resumen

La estimulación celular por medio de la aplicación de campos eléctricos de frecuencia variable constituye un método para modificar características celulares como metabolismo, orientación, migración y función biológica. Para este tipo de estudios y comportamiento, equipo comercial complejo y de alto costo es usualmente utilizado, este generalmente presenta bajo ancho de banda limitando el alcance de los experimentos.

Este trabajo muestra el diseño e implementación de un prototipo para la estimulación eléctrica y medición de impedancia de muestras celulares, caracterizado por su bajo costo, portabilidad y fácil ajuste de frecuencia y tensión eléctrica, lo cual lo hace adecuado para estudios de estimulación e investigación. Además, el trabajo constituye un estudio preliminar para sistemas con mayor ancho de banda, mayor rango de impedancia y más canales de entrada. El dispositivo es diseñado e implementado con el fin de llevar a cabo experimentos de regeneración y apoptosis. Puede generar señales eléctricas de hasta 40 kHz con tensiones entre 0 V y 100 mV, y es capaz de medir impedancias de hasta 1 MΩ. Experimentos de estimulación celular y de medición de impedancia han sido efectuados sobre muestras de levadura, estos resultados son comparados con los obtenidos utilizando el medidor LCR Agilent 4284A.

Palabras clave: Estimulación celular, medición de impedancia, espectroscopia de impedancia, generación de señales, ABBM.

To my dear mother . . .

Acknowledgement

This work was partially supported by the Costa Rica Institute of Technology (ITCR) and Hamburg University of Technology (TUHH). It represents the culmination of 5 years of study to become a Electronic Engineer with Licienciate's Degree. In all this time many people have contributed in different ways to achieve this goal.

I wish to express my sincere thanks to Prof. Dr.-Ing. Wolfgang Krautschneider, Principal of the Institute of Nano- and Medical Electronics, for giving me the opportunity to perform my Bachelor Thesis in this Institution, for providing me with advice and all the materials and resources to carry out this project.

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Most importantly, I would like to express my gratitude to God for being the light that has illuminated my path, for all his support and blessings. I want to thank my family and friends for their motivation and support, special thanks to my mother which unconditional love and support have encouraged me during all this time.

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Chapter 1

Introduction

Impedance spectroscopy (IS) is a technique used to determine the electrical resistance of a sample as a function of the frequency. An alternating voltage is applied to the sample, and the current flow is measured simultaneously. The impedance is calculated by means of the Ohm's Law and then stored as a frequency response plot, with magnitude and phase, or as a Nyquist plot, with a real vs an imaginary part. The dielectric properties of a sample can be extracted from the impedance, since the electrical conductivity is proportional to the real part of the impedance (resistance, R) and the electrical permittivity is obtained from the imaginary part of the impedance (reactance, X).

The Institute of Nano- and Medicine Electronics of the Hamburg University of Technology (TUHH), and the Department of Electronic Engineering of the Costa Rica Institute of Technology (ITCR) work together in a project aimed to the development of an electronic system that has tree main functions: electronic stimulation, electronic characterization, and simultaneously characterization and stimulation of biological samples [1]. The system will enable characterization of cells through electrical impedance spectroscopy methods in a broad frequency range.

Researchers at the TUHH have been using commercial equipment for impedance spectroscopy of biological samples. The Agilent 4284A LCR meter is controlled from a PC using a GPIB cable and a MATLAB interface, and can produce frequency sweeps from 1 Hz up to 1 MHz. The Gamry Interface 1000E is also controlled from a PC using special software from Gamry Instruments, and the frequency range extends from 0.1 Hz up to 1 MHz. These tools have industrial accuracy and are used for validation of results in cellular growth experiments. However they are expensive, require extra equipment and licenses, and they are not easy to transport, limiting the possible fields of application.

The device presented in this thesis has been designed as a first prototype to address the cost, portability, and complexity issues presented in the above tools. It is a device capable to cause stimulation by the application of waveforms with programmable amplitude and frequency, allowing single frequency experiments and also accurate frequency sweeps, necessary for impedance spectroscopy of biological samples. The proposed device constitutes the basis for developing

impedance spectroscopy tools with higher bandwidth, higher impedance range and experiment parallelization since the critical parts of the system can be replaced with high-performance devices to expand the range of measurements.

1.1 Electric stimulator for impedance spectroscopy

The concerned device consists in an electric cell stimulator which works at frequencies up to 40 kHz at voltages from 0 V to 100 mV for impedances up to 1 MΩ. This system will be used to study the growth of cell cultures stimulated with electric fields of adjustable amplitude and frequency. Cells under the influence of electromagnetic fields grow in a different way. Some cell cultures exhibit accelerated reproduction, while other cells can be killed by a specific electric field that induces apoptosis.

The general diagram of the desired system is shown in Figure 1.1. The *Signal generation* block is intended to generate sinusoidal, triangular and square waveforms at frequencies up to 40 kHz. Then the signal goes trough the *Signal conditioning* stage to be filtered and adjusted in amplitude, from 0 V to 100 mV. These low voltage, variable electric fields are applied to the Device Under Test (DUT), in this case biological samples, to cause stimulation. Once the sample is stimulated, the *Signal acquisition* block takes electric measurements of the sample to compute the impedance in the next stage, *Signal processing*. Finally, the impedance is stored in a memory and can be further analyzed to obtain the relevant biological information.

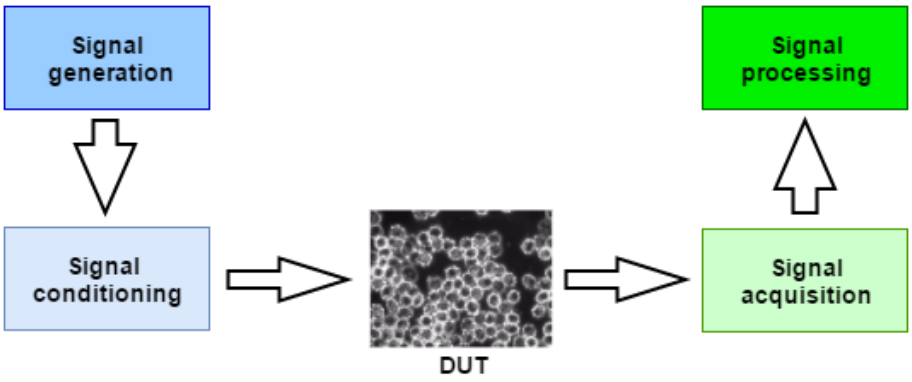

Figure 1.1: Stimulation and impedance measurement system.

The digital processing of the signals is accomplished by DE0-Nano-SoC development board, a System on Chip which integrates a FPGA and a Hard Processor System (HPS). Supplementary circuits for analog processing of the signals are designed and implemented using discrete elements and Integrated Circuits (IC).

1.1.1 General Objective

Design an electronic prototype for cell stimulation in the frequency range up to 40 KHz in order to carry out experiments for monitoring cell cultures growth.

1.1.2 Specific Objectives

- Develop an electronic interface to link up signals between the DE0-Nano-SoC development board, amplifying and filtering tools, and DUT.

- Implement high-level computational algorithms to enable impedance calculation as well as processing of the measured data.

- Carry out experiments using the developed device in order to observe changes in the grow rate of cell samples.

1.2 Document structure

The main content of this thesis is presented in the next five chapters as follows.

Chapter 2 presents the basic theory for understanding the context of the project, as well as its design and implementation. This chapter includes a literature review of the cell response before the application of electric fields, the concept of impedance spectroscopy and some of its applications in the area of biology and medicine. Also, it presents methods for impedance measurement focusing on ABBM.

Chapter 3 presents electric circuits and systems for waveform generation and data acquisition. It includes a short description of the DDS architecture, characteristics of the I2V based on inverting OA, and an overview of the ADC operation, the quantization error, and sampling criteria.

Chapter 4 begins with the design proposals referred to the solution of the concerned problem, then the selected solution is explained in detail by stages. First, the analog implementation is described showing the functions of each block, its operation, and components. Then, the digital implementation explains the designed algorithms for system configuration, communication between DE0-Nano-SoC development board and analog implementation, impedance computation and data

storage.

Chapter 5 shows the experimental results using the physical prototype. It shows the operation of the serial communication algorithm, the frequency response of the filters, results of electric stimulation and impedance measurement of known loads and yeast samples by the application of fixed frequencies and frequency sweeps.

Chapter 6 presents the conclusions of the project. Here is given a brief analysis of the system capabilities and limitations. This chapter also includes some recommendations for further work.

Chapter 2

Impedance spectroscopy and applications

Cells are the basic structural and functional unit of every living organism. Their biological composition is linked to an electric response, changes in their composition leads to changes in electric characteristics like conductivity and permittivity [2]. Reciprocally, modifications in their electric characteristics cause alterations in their metabolism and function. These characteristics become really important in areas like medicine to make electrical differentiation between healthy and unhealthy cells. For example, the membrane fluidity in cancer cells is higher [3].

Impedance spectroscopy is a technique used to determine the electrical impedance of a sample as function of the frequency. The sample is stimulated by application of variable frequency electric fields and the current is measured to obtain the impedance spectrum. This technique is used in biology to carry out toxicological tests, medical diagnosis, cell concentration and stem cell research [1].

The impedance of a sample and its dielectric properties are relevant for a wide range of applications. In biology, a common experiment is the growth of cell cultures under different environmental conditions. The concentration of cells present at a specific point of time can be determined by optical means, by observing the sample under a microscope and staining the cells with a fluorescent marker. However, these markers are often toxic and alter the growth of the cells. By constantly monitoring the impedance of the cells, a researcher can measure the approximate number of cells present in the sample in real time, without damaging the cells in the process.

Another application is the study of the inner part of the cells as a function of the frequency. In literature it is established that most of the animal cells exhibit three dispersion regions, known as the alpha, beta and gamma regions [4]. The alpha region describes the low frequency response of the cell culture, involving the electrode and cellular membrane polarization effects. The beta region is related to the cellular and nuclear membranes, and the internal organelles. The gamma region, observable at frequencies above 10 GHz, describes the water relaxation effect. These three dispersion regions are different between distinct types of cells and can be determined by impedance spectroscopy.

In medicine, Tumor Treating Fields (TTFields) therapy is used to stunt the growth of cancer cells by tuning intensity and frequency of electric fields, exposure of TTFields may stop cell proliferation and causes apoptosis [5]. This method has comparable efficiency with chemotherapy, minimizes toxicity and enables a better quality of life [6]. Others examples related with the regeneration and cell growth consist in applying electrical stimulation to enhance osteogenesis processes [7], and to accelerate nerve and cell regeneration in cell cultures and injury muscles [8].

2.1 Impedance measurement methods

Impedance is the opposition that presents a material to the flow of an alternating current. It is represented by a vector, Z, in polar form with magnitude and phase, as shown in Equation 2.1, or in rectangular form as a complex quantity with real and imaginary part, as shown in Equation 2.2.

$$Z = |Z| * \angle Z \tag{2.1}$$

$$Z = R + jX \tag{2.2}$$

Figure 2.1 shows the representation of the impedance in the complex plane.

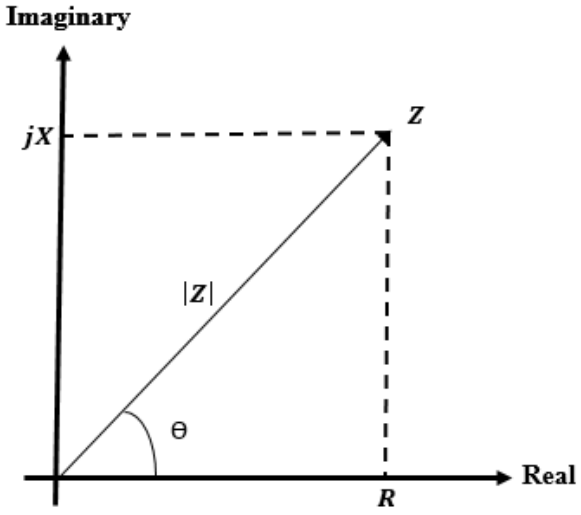

Figure 2.1: Impedance representation in the complex plane.

The imaginary part of the impedance represents the reactance, X, of the material. There are two kinds of reactances, Equation 2.3 shows the expression to compute the inductive reactance, X_L, and Equation 2.4 the one for a capacitive reactance, both as a function of frequency, f.

$$X_L = 2\Pi f L \tag{2.3}$$

$$X_C = \frac{1}{2\Pi f C} \tag{2.4}$$

Where L constitutes the inductance of the material and C the capacitance.

There are many impedance measurement methods, each one presents different advantages and disadvantages in frequency scoped, measurement range, and accuracy.

Bridge method Figure 2.2 shows the circuit for measuring impedance using bridge method. When there is not current flowing in the detector, D, the unknown impedance is obtain from Equation 2.5.

$$Z_x = \frac{Z_1}{Z_2} Z_3 \tag{2.5}$$

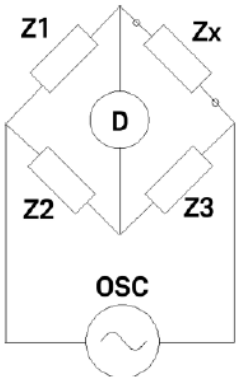

Figure 2.2: Impedance measurement using bridge method [9].

Resonant method In Figure 2.3 the diagram for measuring impedance based on bridged method is shown. The capacitance C is adjusted until get resonance at a known frequency. The frequency, C and Q are used to compute the impedance form by Lx and Rx. Q, the quality factor, is define as the ratio between the energy dissipated and stored, it can be measured in the circuit using a voltmeter.

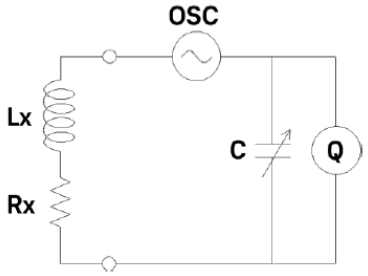

Figure 2.3: Impedance measurement using resonant method [9].

I-V method Figure 2.4 shows the circuit for I-V method. The voltage and current are measured to compute the impedance Zx. The current is computed by Ohm's Law from the voltage in a known low-value resistor R. Equation 2.6 describes this relation.

$$Z_x = \frac{V_1}{I} = \frac{V_1}{V_2} R \tag{2.6}$$

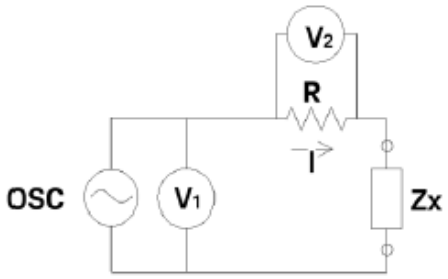

Figure 2.4: Impedance measurement using I-V method [9].

Network analysis method In this method the impedance is obtained from the reflection coefficient. It is computed as the ratio between the incident and reflected signal, these are measured using a network analizer. Figure 2.5 present the diagram for this method.

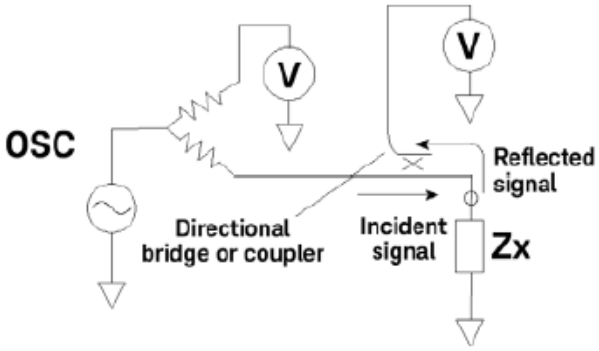

Figure 2.5: Impedance measurement using network analysis method [9].

Auto balancing bridge method (ABBM) Figure 2.6 shows the circuit for this method. It is based on a current-to-voltage converter (I2V), implemented by an operational amplifier (OA) in inverting configuration. The input voltage (Vi) is applied to the Device-Under-Test (DUT), and the generated current is converted into an output voltage (Vo). The gain depends on the feedback resistance (Rr) and on the DUT itself. The impedance is calculated using Equation 2.7

$$Z_{DUT} = -R_r * \frac{V_i}{V_o} \tag{2.7}$$

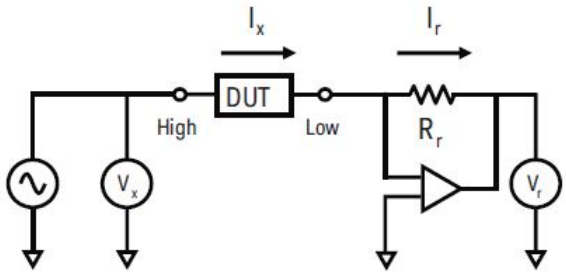

Figure 2.6: Impedance measurement using ABBM [9].

In the current design, the input and output voltages are sampled by ADCs and processed using the Fast Fourier Transform (FFT). The peak voltages at the fundamental frequency are used to calculate the magnitude of the impedance, according to Equation 2.7. The phase difference at the fundamental frequency is equivalent to the phase of the impedance. The processing tasks are accomplished by a DE0-nano-SoC board, a System on Chip which integrates a FPGA and a Hard Processor System (HPS).

Table 2.1 presents the relevant advantages and disadvantages of the reviewed methods.

Table 2.1: Some impedance measurement methods. Adapted from [9].

Method	Advantages	Disadvantages	Aplicable frequency range
Bridge method	-High accurrency. -Wide frequency coverage by using different types of bridges. -Low cost.	-Needs to be manually balanced. -Narrow frequency coverage with a single instrument.	DC to 300 MHz
Resonant method	-Good Q accuracy up to high Q.	-Needs to be tuned to resonance. -Low impedance measurement accuracy.	10 kHz to 70 MHz
I-V method	-Grounded device measurement. -Suitable to probe-type test needs.	-Operating frequency range is limited by transformer used in probe.	10 kHz to 100 MHz
Network analysis method	-Wide frequency coverage from LF to RF. -Good accuracy when the unknown impedance is close to characterisitic impedence.	-Recalibration required when the measurement frequency is changed. -Narrow impedance measurement range.	5 Hz and above
Auto balancing bridge method	-Wide frequency coverage from LF to HF. -High accuracy over a wide impedance measurement range. -Grounded device measurement.	High frequency range not available.	20 Hz to 120 MHz

Since ABBM presents high accuracy in a wide impedance range, operates in a frequency range that suits the requirements of the design, and constitutes a simple method, it represents the best option for impedance measurement in this project.

Chapter 3

Waveform generation and data acquisition

Reliable stimulation of cells for their characterization requires to apply low-voltage, variable-frequency electric fields as a method to avoid cell degradation [10]. The applied electric fields as well as the generated current must be conditioned before being interpreted by the digital system. This chapter shows a review of DDS method for waveform generation, presents the operation principles of the Current-to-Voltage Converter and explains important terminology of the ADC.

3.1 Direct Digital Synthesis

Direct Digital Synthesis (DDS) is a digital method that consist in generating multiple frequency signal from a single frequency source. The basic architecture of a DDS is shown in Figure 3.1. The frequency source acts as a clock for driving the address counter; a Programmable Read Only Memory (PROM) stores the waveform conversion data, every count addresses a digital amplitude value of the waveform. Finally, the digital signal is converted into analog using a Digital to Analog converter (DAC).

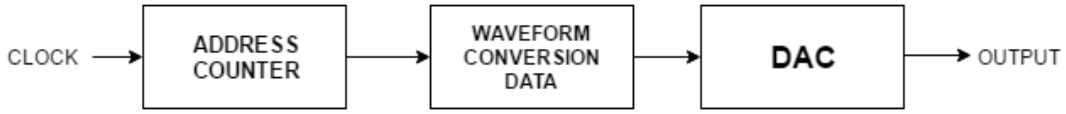

Figure 3.1: Basic architecture of a Direct Digital Syntehesis.

This architecture does not allow changes in the output frequency except when the clock frequency is changed or the PROM is reprogrammed. A more complex architectures is shown in Figure 3.2. It integrates a Numerically Controlled Oscillator (NCO) as a flexible method to generate variable frequency output signals [11].

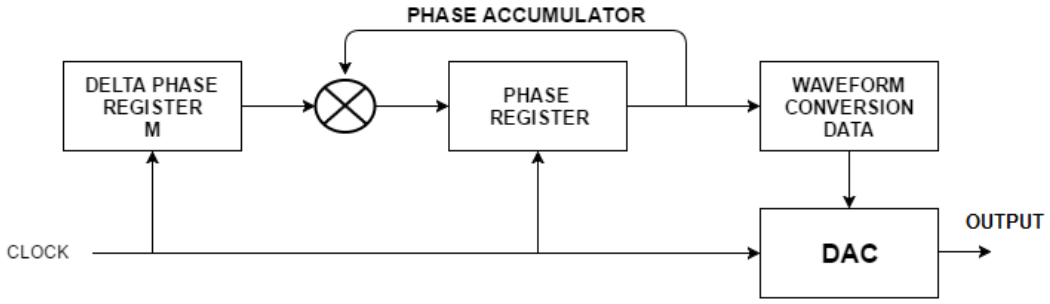

Figure 3.2: Direct Digital Synthesis architecture.

The NCO incorporates a phase accumulator. This sub-system stores the value of phase in a range from 0 to 2 π. Every clock cycle the value in Δ phase register is added to the phase register, and the waveform phase changes accordingly. The value stored in the Δ phase register controls the speed in which the phase of the signal changes. If it decreases the frequency of the output signal also decreases, and if it increases the frequency of the output signal increases too [12].

For a n-bit phase register, 2^n represents the number of points to complete a whole signal cycle. The Equation 3.1 is used to determine the output frequency of the signal base on the value of the Δ phase register. This equation is known as the 'tuning equation'.

$$f_{out} = \frac{M * f_{MCLK}}{2^n} \tag{3.1}$$

With f_{MCLK} as the clock of the system.

3.2 Current-to-Voltage converter

A Current-to-Voltage Converter (I2V) is a device that converts an input current into a proportional output voltage. This behavior can be achieved using a Operational Amplifier (OA) in inverting configuration. The OA configuration is showed in Figure 3.3.

There are two important characteristics of the OA that allows its behaviour as a I2V. Since its input terminals act as an open circuit for current and as a short circuit for voltage, practically all the input current flows trough the feedback resistor (R_f) which causes the generation of a proportional voltage, and since the non-inverter input of the OA is fixed to ground, a virtual ground appears in the inverter terminal, causing the voltage dropped in R_f to be the output voltage (V_o) [13].

Equation 3.2 shows the relationship between the input current and the output voltage.

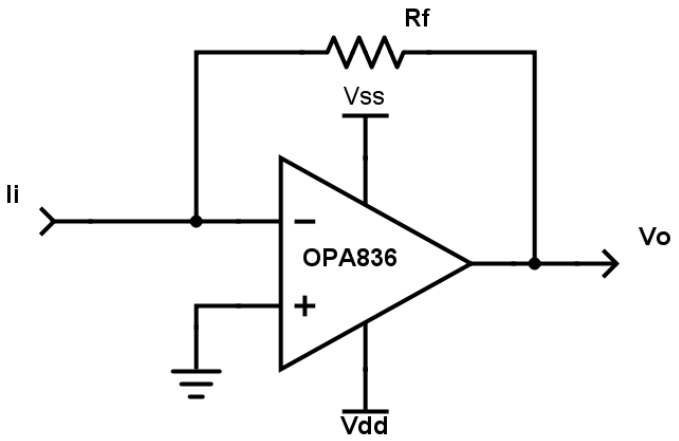

Figure 3.3: Current-to-Voltage Converter.

$$V_o = I_i * R_f \tag{3.2}$$

3.3 Analog-to-Digital converter

An Analog-to-Digital Converter (ADC) is a device that assigns a digital code at the output according with an analog level at the input. Each analog level is attached with a unique code, this is known as quantization and is showed in Figure 3.4. For an N-bit code is possible to get a maximum of 2^N states at the output. The resolution of the ADC indicates how much must change the analog input in order to produce a change of one state in the output, it can be seen as the weight of the Least Significant Bit (LSB).

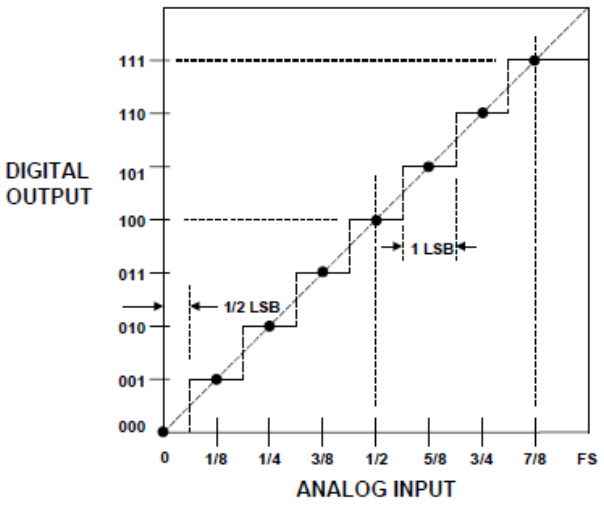

Figure 3.4: Transfer funcion for an ideal unipolar 3-bit ADC [14].

The analog input of the ADC can take any value, however the digital output can not since it is quantized. it a difference of up to ½ LSB between the input and the output, this is called quantization error [14].

The time between each input reading is commonly describe using the sampling frequency, f_s. The Nyquist Criteria establishes that the sampling rate must be at least twice the higher frequency of the input signal. If this criteria is not reached, aliasing errors appear.

In real-time systems, the data processing must be done in an interval of $1/f_s$. In Fourier Fast Transform (FFT) applications a package of data is read and stored in memory. When the package is full the FFT is calculated and at the same time a new package is loaded to memory. The FFT must be calculated before the next package be loaded to the memory.

In systems when the input signal change more than one LSB during the data conversion large errors can be got. It happens in signals that change in time, like in AC signals. Most modern ADCs have a sample-and-hold amplifier (SHA) in order to process AC signals, these are known as sampling ADC. The SHA samples the input during sampling mode and hold its value during hold mode [15].

Chapter 4

Design of a low-frequency cell stimulator

The first section of this chapter presents different options for the implementation of the impedance spectroscopy device: One based on a NI sbRIO-9651 system on module, the second based on Peripheral Component Interconnect eXtension for Instrumentation (PXI) of National Instruments, and an implementation using DE0-Nano-SoC development board. The second part describes the selected architecture, it shows the block diagram of the system and gives a detailed explanation of each functional blocks: waveform generation, signal conditioning, impedance measurement circuit and low-pass filters. Finally, the third part includes the digital logic and programming required for calculating the impedance from the voltage measurements.

4.1 Design options

The concerned device is designed to cause cellular stimulation and measure the resultant impedance. The cellular stimulation is achieved by the appliance of sine, triangular and square waveforms with amplitudes up to 100 mV and frequencies up to 40 kHz. Impedance calculation requires to measure the input and output voltage of the DUT based on the ABBM method. Three design proposals had been consider in order to achieve this behaviour.

The first approach consist in using a NI sbRIO-9651 System on Module (SOM) board, a specially designed platform for control and monitoring applications. It integrates a real-time processor, a reconfigurable FPGA, and analog and digital input/outputs. This device is used for FFT algorithm implementation, impedance computation and storage. It requires an analog system for data conditioning and acquisition.

A second approach consist in a system based on Peripheral Component Interconnect eXtension for Instrumentation (PXI). This is a PC-based platform for developing test, measuring and control systems [16]. It consists of a chassis with integrated timing and synchronization, input/outputs PXI

modules, and an in-chassis embedded computer. The PXI modules required for this application are: a Sampling System for Data Acquisition (DAQ) and a Waveform Generator System. The whole system is controlled by NI LabView, a software development environment for measurement and automation.

The third option consist in using DE0-Nano-SoC development board which incorporates a FPGA, a HPS, General Purpose Input/Outputs, memory devices, a 8-channel ADC, among others. This device is used for configuring the stimulation, taking the digitized samples for FFT computation, computing the magnitude and phase of the impedance and storing the data. As in the first case, it requires an analog system for data conditioning and acquisition.

All options have the proper hardware to achieve the electric requirements. However, in terms of cost second option is discarded due to it constitutes the most expensive system, the total cost can be up to some thousand euros, on the other hand, the third option is the cheaper, the cost of a DE0-Nano-SoC development board is not higher than €100. In terms of size, the first and third options have the smallest dimensions, making them suitable for being easily transport. Therefore, the third option is the one that best meets the design requirements: low-cost, portability and easy reconfigurability of frequency and voltage. It is important to mention that the Institute already have one available for the project.

4.2 Impedance spectroscopy device based on SoC

Figure 4.6 shows the functional block diagram of the proposed system. It consists of an analog implementation for data conditioning and acquisition, and a digital implementation intended to configure the stimulation parameters, take packages of samples and apply them the FFT for calculation of the impedance spectrum.

4.2.1 Waveform generator

The *waveform generator* block is intended to generate sinusoidal, triangular and square waveforms at frequencies up to 40 KHz with magnitudes between 0 V and 100 mV. The waveform, frequency and phase shift are configured by the DE0-Nano-SoC board allowing sample stimulation by a fixed frequency signal or frequency sweeps. There have been considered three different options to perform this task.

The first option is to use the FPGA contained in the DE0 Nano SoC to generate all this signals digitally, and then use a DAC to get analog signals with the required specifications. Using the FPGA, digital signals with different waveform, amplitude and frequency can be generated. These signals

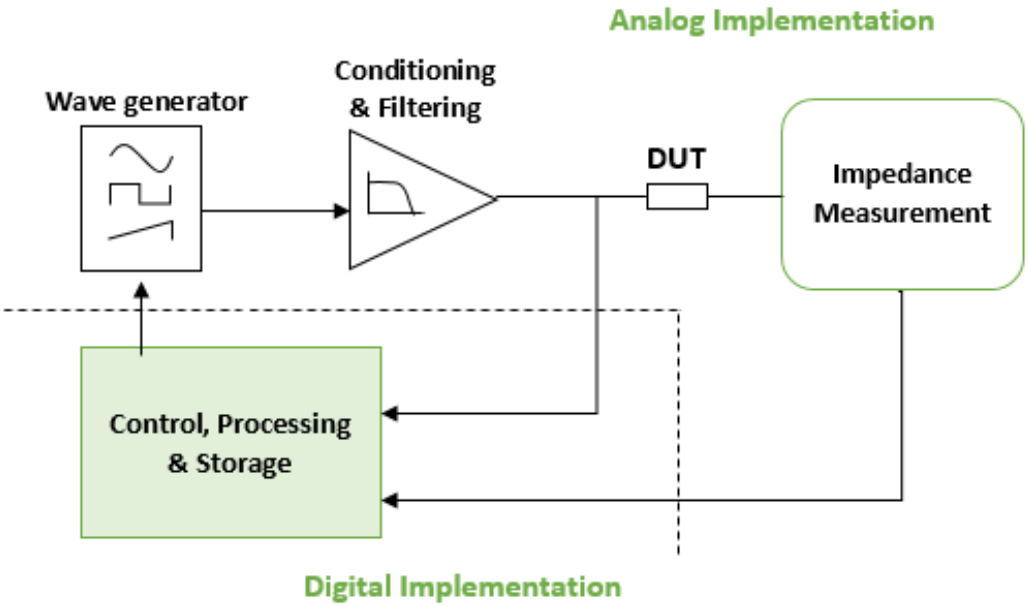

Figure 4.1: Functional block diagram of the low-frequency cell stimulator.

have low voltage boundary of 0 V and a high voltage boundary of 3.3 V. The sinusoidal waveform is commonly stored in a ROM inside the FPGA, and would be transmitted to the DAC either by parallel or serial communication.

The second option implies to use a Voltage-Controlled Oscillator (VCO), it is a device capable to generate output signals according to the input voltage applied. MAX038 is a high-frequency VCO that generates triangle, sawtooth, sine, square and pulse waveforms with frequencies from 0.1 Hz to 20 MHz. However, it is necessary to use a simple DAC to control the VCO using the DE0-Nano-SoC development board.

The third approach consists in using a Direct Digital Synthesis (DDS). Basically, it is a device that produces analog waveforms through the conversion of time-varying digital signals into analog using an integrated DAC [19] (for more information see chapter 3). As in above options, DE0-Nano-SoC board is programmed to adjust the waveform and frequency of the signal.

The characteristics of the third implementation make him the best option to generate analog signals with variable output frequencies due to:

- Flexible tuning, just requires to write some internal registers by serial protocol for waveform, frequency and phase adjustment.
- Eliminates the need of extra algorithms for signal construction, its architecture is optimized to build sine, triangular and square signals.
- Al thought it require an extra element for adjusting the amplitude, it can be achieved with simple

components.

Table 4.1 presents a list of DDS ICs and a brief description of their relevant characteristics.

Table 4.1: DDS options

Chip	Freq Range	Freq Resolution	Waveforms	IC Pins
AD5932	Up to 25 MHz	24 bits	Sine, triangular, square	16
AD9833	0.1 Hz - 12.5 MHz	28 bits	Sine, triangular, square	8
AD9838	0.06 Hz - 8 MHz	28 bits	Sine, triangular	20
AD9850	Up to 62.5 MHz	32 bits	Sine, square	28

Due to size, resolution, and waveform characteristics the AD9833 is chosen to be implemented in the target application.

4.2.2 Conditioning & filtering

The *conditioning & filtering* block adjusts the amplitude of the signal in a range from 0 V to 100 mV, it also incorporates a LPF in order to decrease the effects of noise and spurious signals.

Amplitude and filter conditioning architectures require the use of OA. Table 4.2 presents a list of OA and a brief description of their relevant characteristics.

Table 4.2: OA options

Chip	Supply range (V)	GBP (MHz)	Slew Rate (V/us)
OP284	2 - 36	4.25MHz	4
AD820	5 - 30	1.9MHz	3
OP213	4 - 36	3.4MHz	1.2
OPA2365	2.2 - 5.5	50 MHz	25
OPA2836	2.5 - 5.5	205 MHz	560

Gain Bandwidth Product (GBP) and slew rate characteristics make the OPA2836 the best option for the current design.

4.2.3 Impedance measurement

The *impedance measurement* block contains the hardware required for the impedance measurement method. For ABBM, this block consists of a current-to-voltage converter. The OA used to implement the I2V is the same as the one described for the low-pass filters.

4.2.4 Control, processing & storage

Control, processing & storage block is intended to carry on the waveform, frequency and phase shift signal configuration, as well as execute the stimulation process by a single frequency or frequency sweep. It also samples the DUT input and output voltages and computes the FFT. It extracts the magnitude information from the fundamental frequency of the signals and calculates the impedance. Finally, it stores the impedance data in a text file for further analysis.

The entire block is implemented in the DE0-Nano-SoC development board. This device is programmed using Quartus Prime Software, a design environment that allows to program the FPGA using a Hardware Description Language (HDL), and interconnect internal elements such as GIOP, ADC, and HPS by the system integrator tool, Qsys.

4.3 Analog frontend

4.3.1 Waveform generation

The AD9833 is a DDS optimized to act as a programmable waveform generator that can produce sine, triangular and square wave outputs with output frequencies up to 12.5 MHz. It has a 0.1 Hz resolution and is programmed using 3-wire serial interface. The disadvantage of this chip is that has an output amplitude of around 650 mV for sine and triangular waves and 3.3 V for square waves, what makes necessary to use an attenuator at the output to get a variable amplitude between 0 and 100 mVpp.

Figure 4.2 shows the electric diagram for the Programmable Waveform Generator. MCLK, SDATA, SCLK and FSYNC are serial protocol terminals use to stablish communication between AD9833 and DE0-Nano-SoC development board.

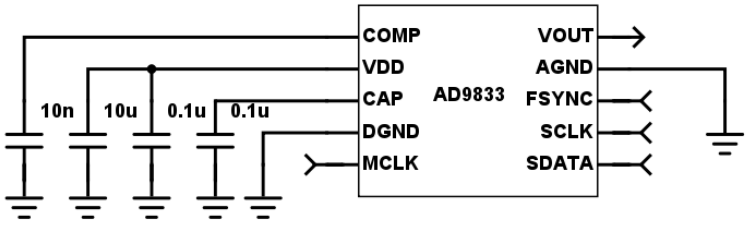

Figure 4.2: Electric diagram of the Programmable Waveform Generator.

4.3.2 Voltage regulator

Initially, the design was supposed to work with positive voltages due to DE0-Nano-SoC board limitations. However, this implementation increase noise, biasing and distortion issues [21]. Thus, a

double-supply system is implemented making necessary to use a method for get a negative supply.

The TL7660 is a Voltage Converter IC that uses two external capacitor for charge pump and charge reservoir functions, this allows conversion of positive voltages into negatives. Figure 4.3 shows the electric diagram for the Voltage Regulator.

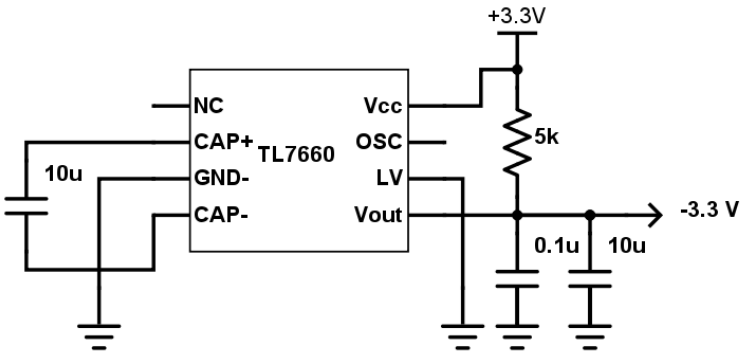

Figure 4.3: Electric diagram of the Voltage Regulator

When this IC is powered with +3.3 V, theoretically, the output is a DC signal of -3.3 V.

4.3.3 Attenuator

The attenuator is intended to decrease the signal amplitude in the range of 0 V to 100 mV. Using an Operational Amplifer in inverting configuration is a simple form to get an attenuator, Figure 4.4 shows the electric diagram for this implementation.

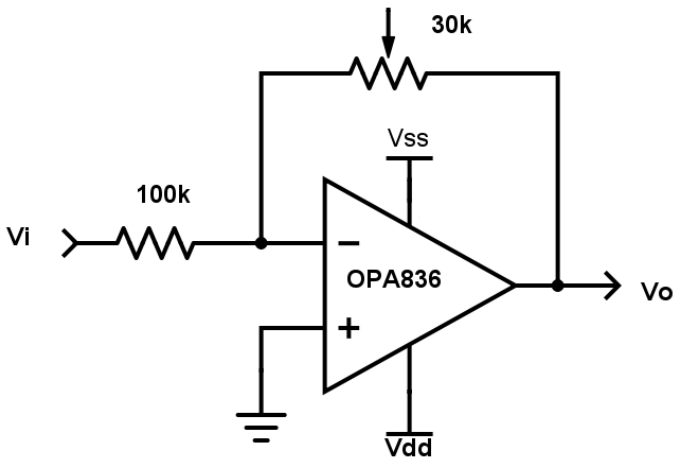

Figure 4.4: Electric diagram of the Attenuator

This circuit allows a minimum attenuation factor of 0.3.

4.3.4 Low-pass filter

The presence of noise and spurious signals in digital systems is inevitable. The repetition rate, rise and fall times, amplitude and waveform of the signals in the system cause the increase of energy in many points of the frequency spectrum [22]. This makes necessary to add a Low-Pass Filter (LPF) to attenuate the unwanted signals.

Figure 4.5 shows a Multiple-Feedback architecture for a second order LPF with a cut-off frequency $f_c = 16MHz$.

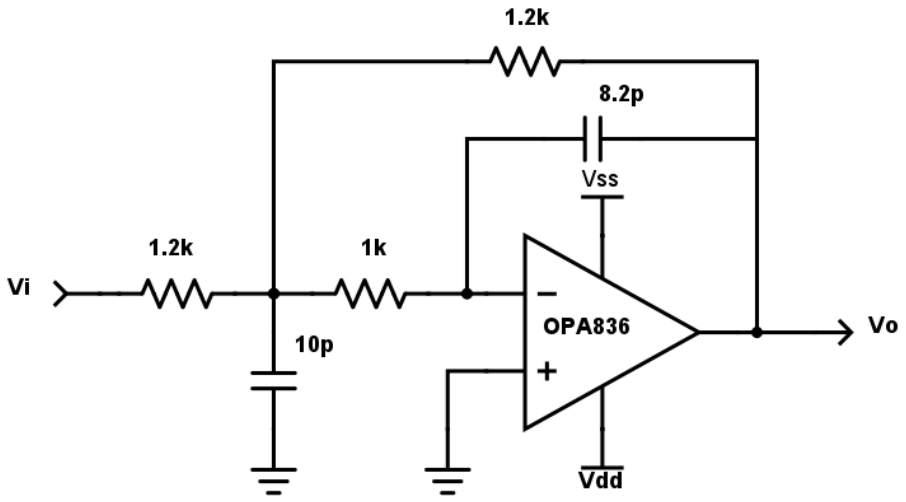

Figure 4.5: Electric diagram of the Low-Pass Filter

4.3.5 Current-to-Voltage converter

The current at the input of the I2V converter can be estimated using Ohm´s Law. With the stimulation voltage as V_i and DUT as the impedance at the input, equation 3.2 turns into 4.1.

$$\frac{V_o}{V_i} = -\frac{R_f}{DUT} \tag{4.1}$$

Equation 4.1 is the same equation use for compute gain in an inverter amplifier. In order two keep attenuation no grater than 10, the feedback resistor must be kept in the same order of magnitude as the DUT, otherwise the attenuation could cause inaccurate calculations. The value of the feedback resistor must be enter during the stimulation configuration in the user interface.

4.3.6 Coupling capacitor

A coupling capacitor is introduced at the output of the attenuator and I2V converter in order to eliminate DC offset voltages. The coupling capacitor in series with the circuit resistance acts as a High-Pass Filter (HPF).

4.3.7 Complete analog circuit

Figure 4.6 shows a general view of the system. The Programmable Waveform Generator is configured by the DE0-Nano-SoC development board using serial protocol. This configuration process establish the waveform, frequency and phase shift of the signal generated by the waveform generator. Then, the signal is attenuated and filtered before being applied to the DUT, this voltage is sampled by the ADC 0. The current flowing through the DUT is converted into voltage using the I2V. This voltage is filtered again for being sampled by the ADC 1. Finally, the DE0-Nano-SoC apply the FFT to the samples and computes the impedance.

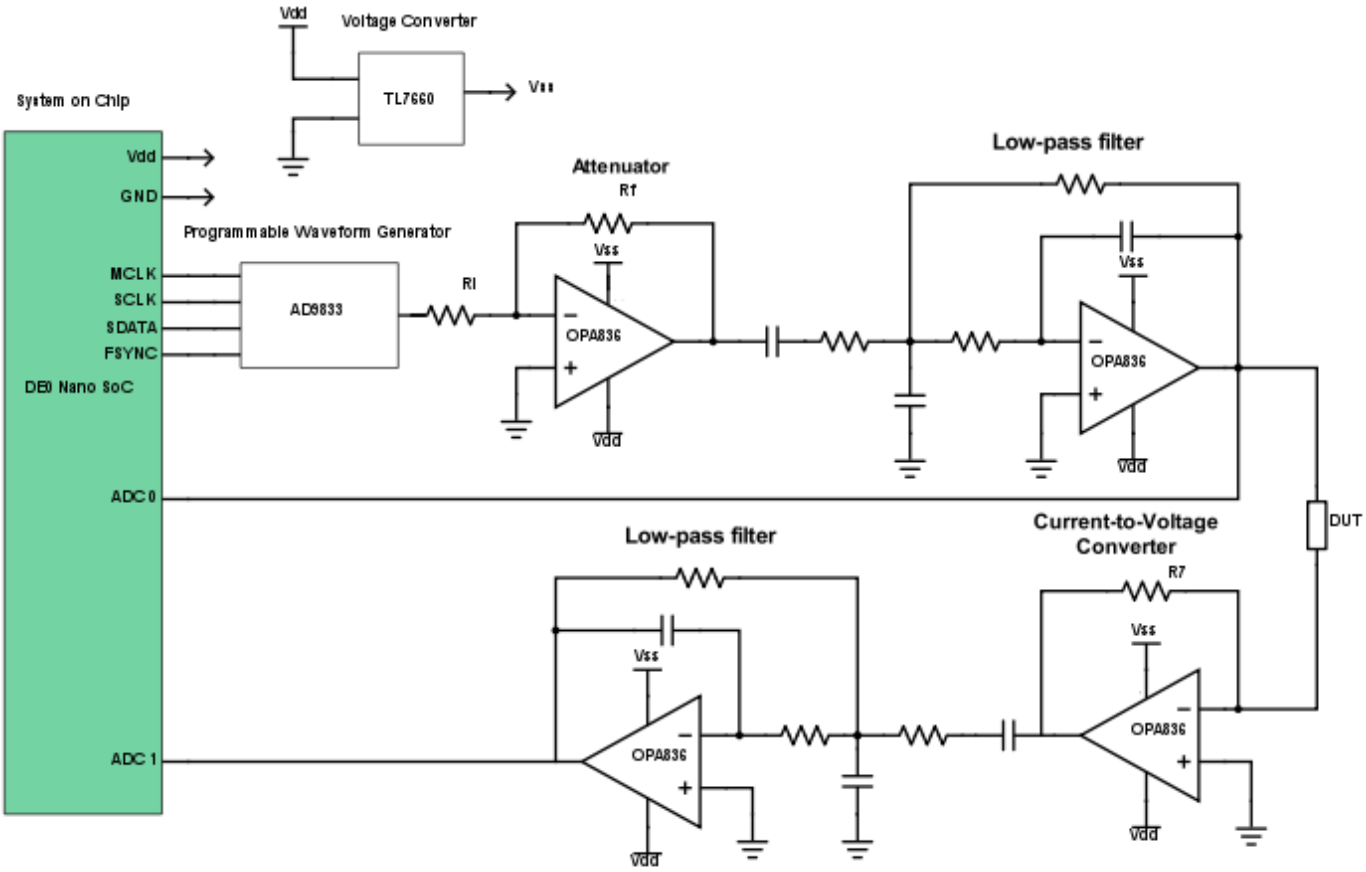

Figure 4.6: Functional block diagram of the low-frequency cell stimulator.

The detailed electric diagram, as well as the PCB layout of this implementation is shown in Appendix C. This appendix also includes a description, the electric diagram and PCB layout of a second prototype. This second device was design with almost the same architecture used in the first prototype. The only difference is that it includes external ADCs with higher sample rate in order to increase the bandwidth of the system. However, due to time restrictions the implementation with this design has not been incorporated in this work.

4.4 Digital design

4.4.1 Waveform generator controller

The HPS of the DE0-Nano-SoC development board include a Dual-core ARM Cortex-A9 processor which has been preconfigured to run Linux. A python script is executed on this image in order to generate a user interface and configure the stimulation process according to the user preferences, feedback resistor, operation mode, frequency, phase shift and waveform. This task requires to interconnect the HPS and the FPGA using internal HPS peripheral bridges. However, the program running on Linux do not have a direct link to the peripheral address, therefore it is necessary to map the physical address to a user space and access the internal registers of FPGA [20]. The Figure 4.7 shows this relationship.

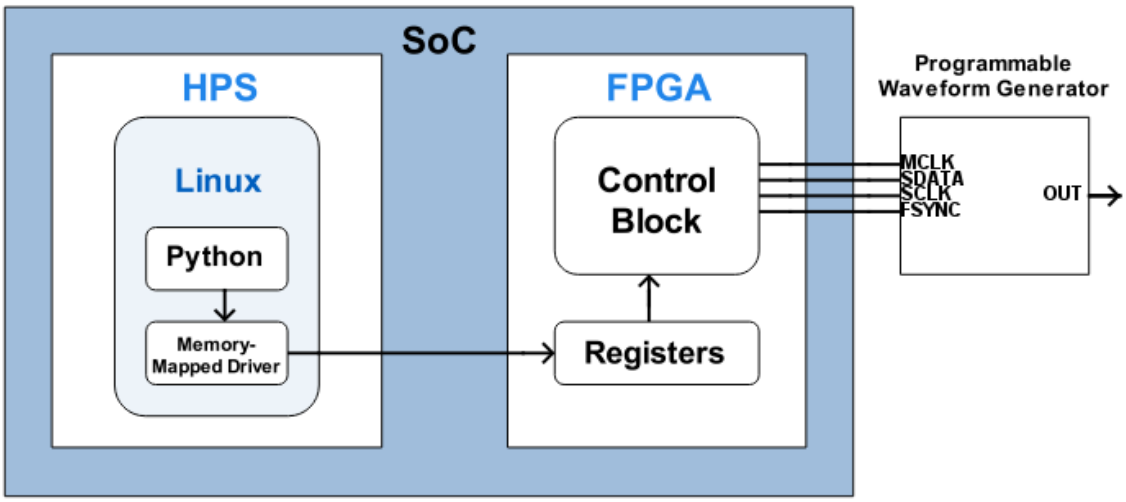

Figure 4.7: Communication between FPGA and HPS.

Once the user introduces and selects the stimulation parameters, the software computes the register values for tuning the waveform generator. There are five 16-bit required transmissions and three configuration registers.

Control register: This register is used to configure the operation of the AD9833. In the first transmission a 16-bit word [0010 0001 00X0 X0X0$_b$] is loaded to the control register in order to: indicate to the AD9833 that control register is going to be written (bits 15 and 14), two consecutive write operations for load the frequency register are required (bit 13), FREQ0 is the register used to write the value of frequency (bit 11), PHASE0 is the register used to write the value of phase shift (bit 10), reset the internal registers before writing them (bit 8), and select the waveform (bits 5, 3 and 1). Table 4.3 shows the state of bits 5, 3 and 1 for configuring the signal waveform.

At the fifth transmission, this register is written again with a 16 bit exit word. The word is the same as the first one except by the reset bit which is set to 0.

Table 4.3: Waveform configuration

BIT 5	BIT 3	BIT 1	Waveform
0	X	0	Sinusoid
0	X	1	Triangule
1	1	0	Square

Frequency register FREQ0: This register stores the data for frequency adjustment. It needs two write operations for load a 28-bit frequency resolution word.

From equation 3.1, the word loaded to the FREQ0 register is calculated as shown in 4.2.

$$FREQ0 = \frac{f_{out} * 2^{28}}{f_{MCLK}} \tag{4.2}$$

The first write operation is used to load the 14 LSB and the second is used to load the 14 MSB. Bit 15 and 14 of each write operation are set in $[01_b]$ to indicate that FREQ0 is been written.

Phase register PHASE0: It stores the desired phase shift, its content is load to the phase accumulator. The word load to this register is computed using equation 4.3.

$$PHASE0 = \frac{PhaseShift * 2^{12}}{2\pi} \tag{4.3}$$

The 4 MSB indicates that PHASE0 register is selected. The remaining 12 bits carry the value computed in 4.3.

The transmissions are accomplish serial protocol. The time diagram of this protocol is shown in figure 4.8. SCLK is used to introduce the serial clock that controls the data load, FSYNC enables the read of data, SDATA contains the data transmitted, and MCLK is the AD9833 internal clock, output frequency is expressed as a fraction of this clock. MCLK and SCLK are connected to a 25 MHz clock generated by the DE0-Nano-SoC board.

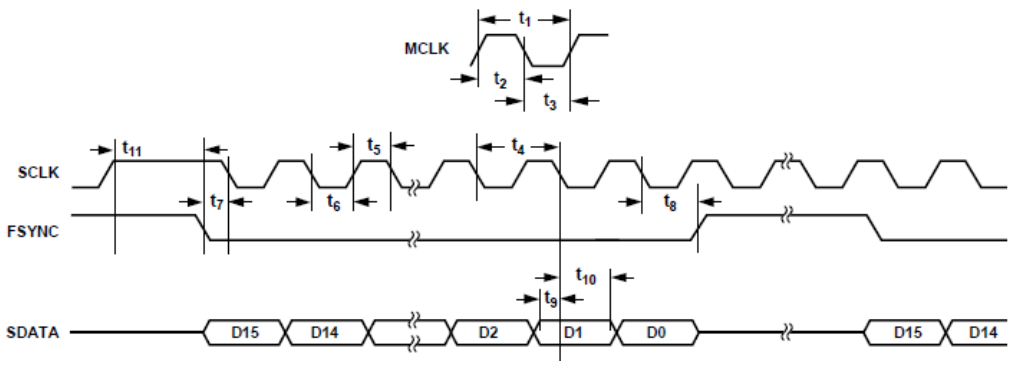

Figure 4.8: Time diagram for serial protocol [12].

Each parameter of the serial protocol has time restrictions, in figure 4.8 they are referred as t_s. Table 4.4 shows these timing characteristics.

Table 4.4: Serial protocol timing characteristics [12].

Parameter	Limit	Unit	Description
t_1	40	ns min	MCLK period
t_2	16	ns min	MCLK high duration
t_3	16	ns min	MCLK low duration
t_4	25	ns min	SCLK period
t_5	10	ns min	SCLK high duration
t_6	10	ns min	SCLK low duration
t_7	5	ns min	FSYNC to SCLK falling edge setup time
t_8 min	10	ns min	FSYNC to SCLK hold time
t_8 max	t_4 - 5	ns max	
t_9	5	ns min	Data setup time
t_{10}	3	ns min	Data hold time
t_{11}	5	ns min	SCLK high to FSYNC falling edge setup time

A module for data transmission is programmed and executed by the FPGA using Verilog (this module is presented on Appendix B). It send the content of the internal registers to the Programmable Waveform Generator IC using the serial protocol described in figure 4.8. The LSB of Configuration Register is used to restart the module and begin a new transmission.

4.5 Impedance calculation

In chapter 2, some methods of impedance measurement were reviewed. ABMM was selected for this application due to its accuracy and frequency response. Using this method implies to sample the voltage applied to the DUT, as well as its resultant current. The resultant current is converted into voltage using a I2V converter, then both voltages are digitized using the ADCs integrated on DE0-Nano-SoC development board.

The software running on the HPS reads packages of 1024 samples and computes the FFT using the NumPy library of Python, this code is showed in Appendix B. When the FFT is computed, the software extracts the DC levels and look for the fundamental frequency component, then calculates the impedance. The computed impedance is stored in a file for further analysis.

Chapter 5

Low-frequency cell stimulator response

This chapter shows the experimental results obtained from the low-frequency cell stimulator device. The operation of the serial protocol as well as the data acquisition elements is showed. Also, it presents experiments carried out on known impedances and yeast cultures.

5.1 Waveform generation

Figure 5.1 shows readings of the MCLK, SCLK, SDATA and FSYNC control signals produced by the FPGA. The process shows a transmission of a 210 kHz triangular signal as follows:

- WORD 1: $[0010\ 0001\ 0000\ 0010]_b \rightarrow$ Configure a triangular signal.
- WORD 2: $[0100\ 0001\ 1000\ 1001]_b \rightarrow$ LSB of a 210 kHz signal.
- WORD 3: $[0101\ 0101\ 1000\ 0001]_b \rightarrow$ MSB of a 210 kHz signal.
- WORD 4: $[1100\ 1010\ 1010\ 1011]_b \rightarrow$ Phase shift of 240°.
- WORD 5: $[0010\ 0000\ 0000\ 0010]_b \rightarrow$ End configuration.

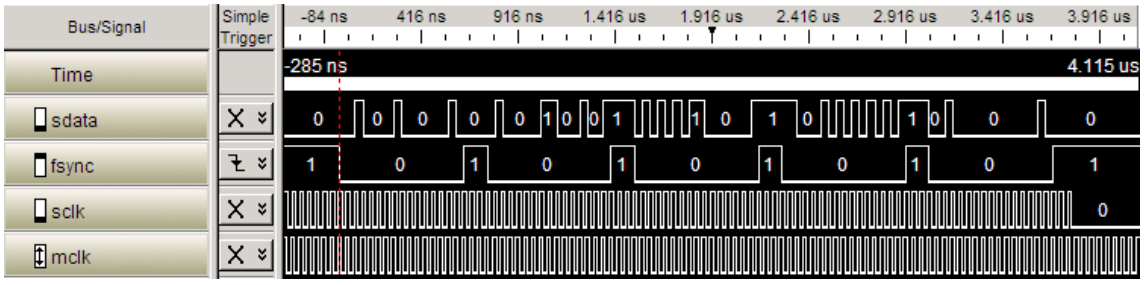

Figure 5.1: Serial Protocol Verification.

The timing characteristics had been measured for the signals in Figure 5.1. This information is shown in Table 5.1.

Table 5.1: Timing measurements of serial protocol.

Parameter	Measurement
t_1	40 ns
t_2	20 ns
t_3	20 ns
t_4	40 ns
t_5	20 ns
t_6	20 ns
t_7	12.5 ns
t_8	27.5 ns
t_9	12.5 ns
t_{10}	27.5 ns
t_{11}	7.5 ns

The verification shows that the four variables of control in the serial protocol meet the requirements on time and the transmission is done properly.

Tests on the Programmable Waveform Generator show that the system interacts properly with the DE0-Nano-SoC development board. Also, the experimental results reveal that the device is capable to produce sine, triangular and square signals with frequencies beyond 1 MHz, which exceeds the 40 kHz target. Oscilloscope captures that shows this feature are presented in Appendix A.

5.2 Signal acquisition

5.2.1 Low-pass filter

Using a Spectrum Analizer, the frequency spectrum of the system is observe in order to locate high energized spurs and harmonics. Figure 5.2 shows the frequency spectrum at the output of the Programmable Waveform Generator. The characteristics of the applied signal are:

- Waveform = sine.
- Frequency = 12 MHz.
- First energized spur $\approx$ 38.19 MHz

The results of this analysis exhibit the presence of noise in the spectrum. This indicates the need of a LPF in order to attenuate this signals, a cut-off frequency of 16 MHz must be enough to deal with the noise. The electric diagram of a LPF with $f_c = 16MHz$ was showed in chapter 5, however,

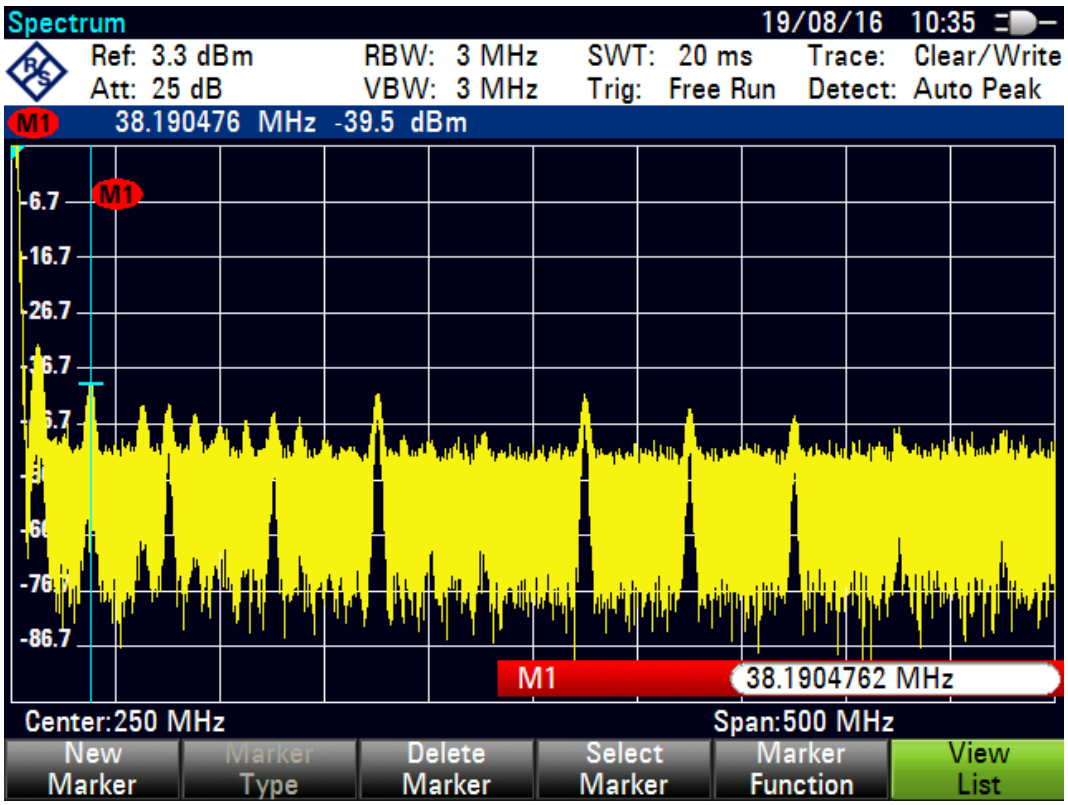

Figure 5.2: Frequency spectrum at the output of the Programmable Waveform Generator

the calculations in this section were theoretical and did not include variations caused by other stages.

Running simulations of the design on TINA-TI, a simulation tool from Texas Instruments, the components were adjusted to get a cut-off frequency as close as possible to 16 MHz. Nevertheless it was not possible to achieve such frequency due to limitations in the components of the circuit. The electric schematic of the simulated circuit is shown in Figure 5.3.

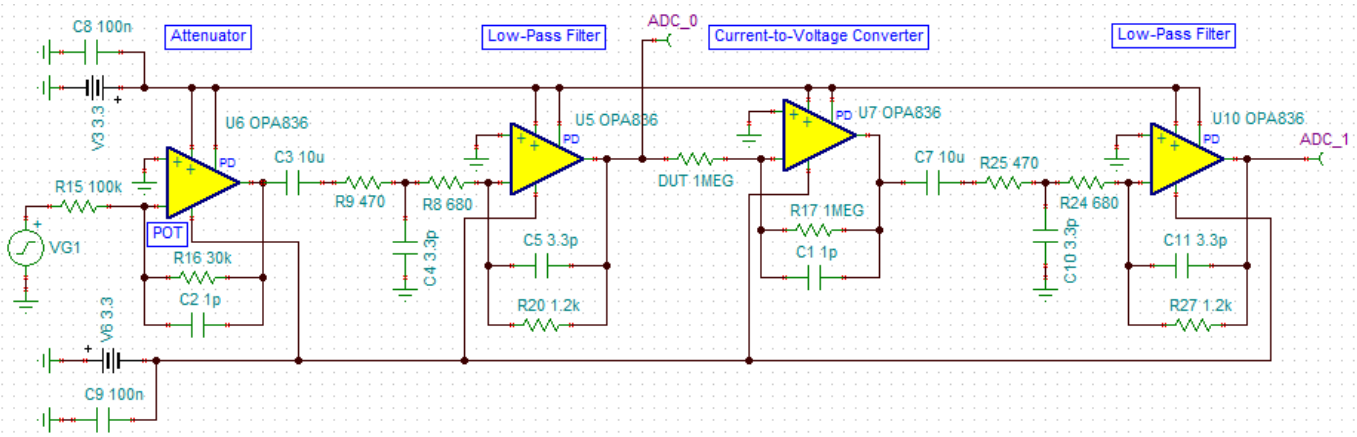

Figure 5.3: Electric schematic from TINA simulation tool.

The simulated frequency response for the circuit of Figure 5.3 is shown in Figure 5.4. The filter response is affected by the impedance used as feedback resistor in the attenuator and I2V, the presented results contemplate a critical operation. Notice that for this case the attenuator is introducing a gain of around -10 dB.

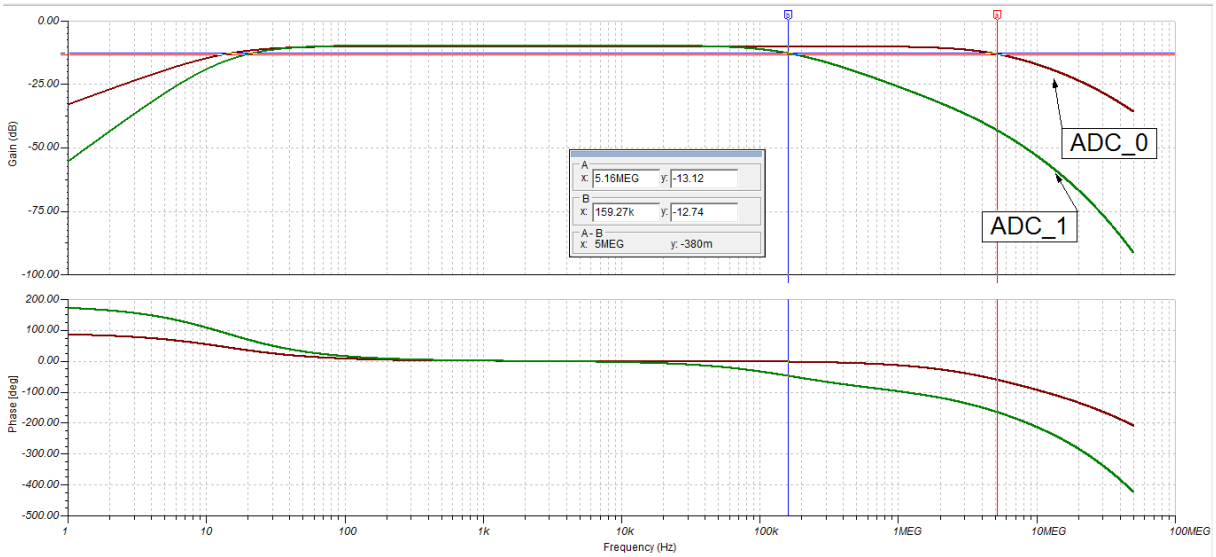

Figure 5.4: Simulated frequency response of the circuit.

The real response of the assembled filters is shown in the next diagrams. For ADC_0 filter the cut-off frequency is 5 MHz and for ADC_1 filter it drops to 57 kHz.

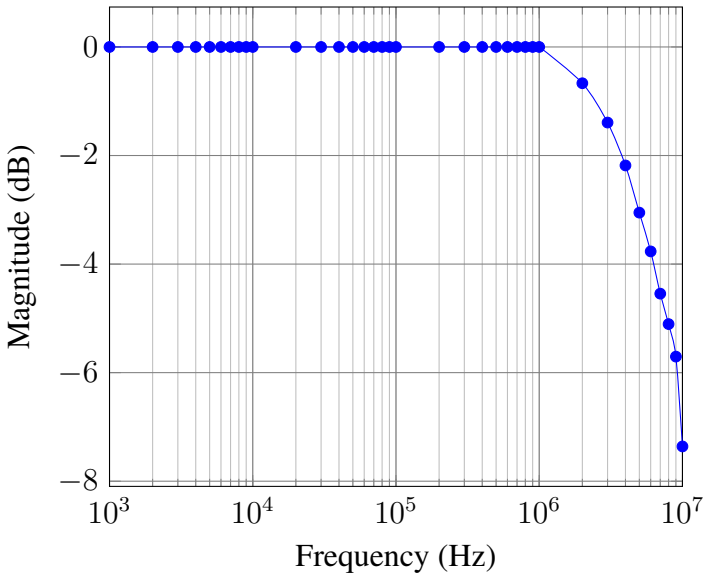

Figure 5.5: Frequency spectrum for ADC_0 filter.

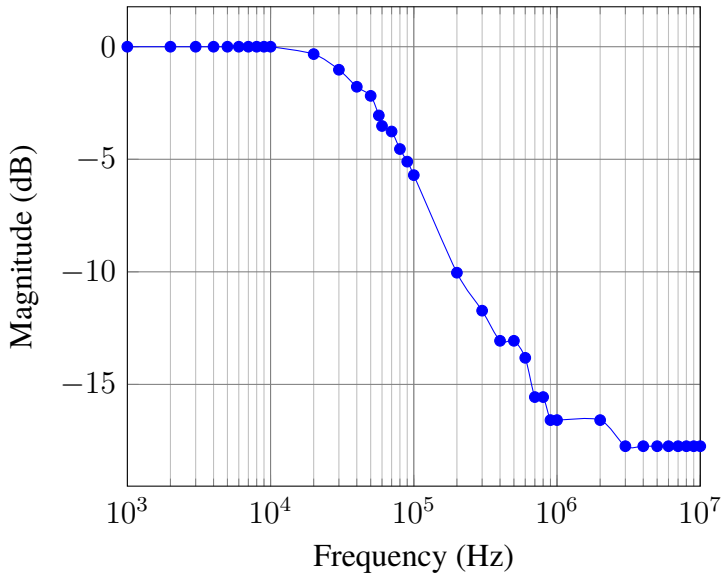

Figure 5.6: Frequency spectrum for ADC_1 filter.

5.3 Impedance measurement

This section presents the results obtained from experiments using known impedances values and yeast cell cultures. Single frequency and frequency sweeps were applied to known impedance loads in order to determine the accuracy of the device. Besides, yeast samples were stimulated using a single frequency in order to observe the growth of the cultures over time, this data is compare with obtained results using the Agilent 4284A LCR meter.

5.3.1 Correction factor

In order to obtain more accurate results it is necessary to add a correction factor to the phase data. This correction factor depends on the frequency and is cause by the fact that the measurements are carried out by one ADC.

The ADC integrated on the DE0-Nano-SoC development board has 12-bit resolution, 500 ksps sample rate and 8-channel analog input. For the concerned application, two of the channels are required, one for measuring the voltage applied to the DUT and other for measuring the output voltage. Due to one ADC must sample two channels, it is impossible to sample them at the same time which cause a delay in the sampling. This delay causes a phase shift between the signals, and it is seen like a reactance by the software that computes the impedance.

Using the linear response of resistors it is possible to estimate the correction factor by applying a frequency sweep to a resistor and obtaining the phase in each frequency. Nine phase data packages were obtain from stimulating three different resistors at frequencies from 100 Hz to 125 kHz with

increments of 100 Hz. The data were average and a third-order median filter were apply to remove peaks and noise. This process were carried out using Matlab software, Figure 5.7 shows the correction factor plot.

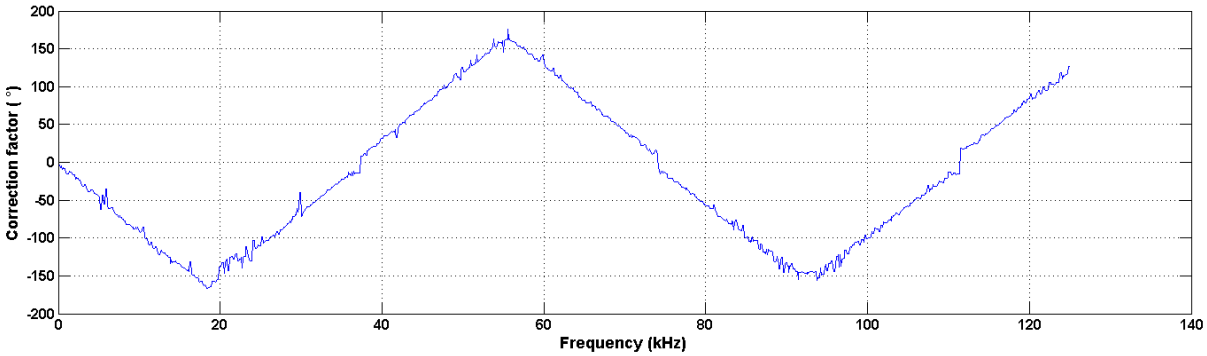

Figure 5.7: Correction factor for phase adjustment.

5.3.2 Stimulation with a single frequency

In order to determine the accuracy of the device, known impedances were stimulated by a single frequency. These impedances were composed by a 10 kΩ resistor in series with a capacitor. Table 5.2 presents the error percentages for phase and magnitude by stimulating impedances with a sine-wave at 40 kHz and 100 mV.

Table 5.2: Stimulation of known impedance by applying a signal of 40 kHz.

C (pf)	**Xc (Ω)**	**Theor. Magnit.**	**Theor. Phase**	**Meas. Magnit.**	**Meas. Phase**	**% Error Magnit.**	**% Error Phase**
10	397887.36	398013.00	-88.56	387550.95	-84.47	2.63	4.62
47	84656.88	85245.46	-83.26	85452.26	-82.67	0.24	0.71
100	39788.74	41026.13	-75.89	39623.77	-74.67	3.42	1.61
220	18085.79	20666.30	-61.06	21542.85	-60.11	4.24	1.55
470	8465.69	13102.21	-40.25	12987.48	-38.93	0.88	3.27
2100	1894.70	10177.91	-10.73	10250.31	-10.66	0.71	0.67

The data in Table 5.2 shows that the device is capable to compute impedance magnitude and phase at frequencies up to 40 kHz with error percentages lower than 10%.

The previous experiment were repeated using the same values of impedance as DUT but with the stimulation frequency set to 100 kHz. The results are showed in Table 5.3.

Table 5.3: Stimulation of known impedance by applying a signal of 100 kHz.

C (pf)	Xc (Ω)	Theor. Magnit.	Theor. Phase	Meas. Magnit.	Meas. Phase	% Error Magnit.	% Error Phase
10	159154.94	159468.79	-86.40	172322.4	-78.59	8.06	9.05
47	33862.75	35308.44	-73.55	38894.9	-73.52	10.16	0.03
100	15915.49	18796.35	-57.86	20216.37	-56.98	7.55	1.52
220	7234.32	12342.42	-35.88	14063.8	-36.49	13.95	1.68
470	3386.28	10557.79	-18.71	11702.32	-18.12	10.84	3.15
2100	757.88	10028.68	-4.33	11034.7	-4.39	10.03	1.29

As can be observed in Table 5.3, the device can operate in frequencies up to 100 kHz but with a slightly increment of error that exceeds the goal of 10%.

Next experiment consisted in stimulating yeast cultures by the appliance of a sine-wave. Figure 5.8 shows a picture of the setup of the experiment.

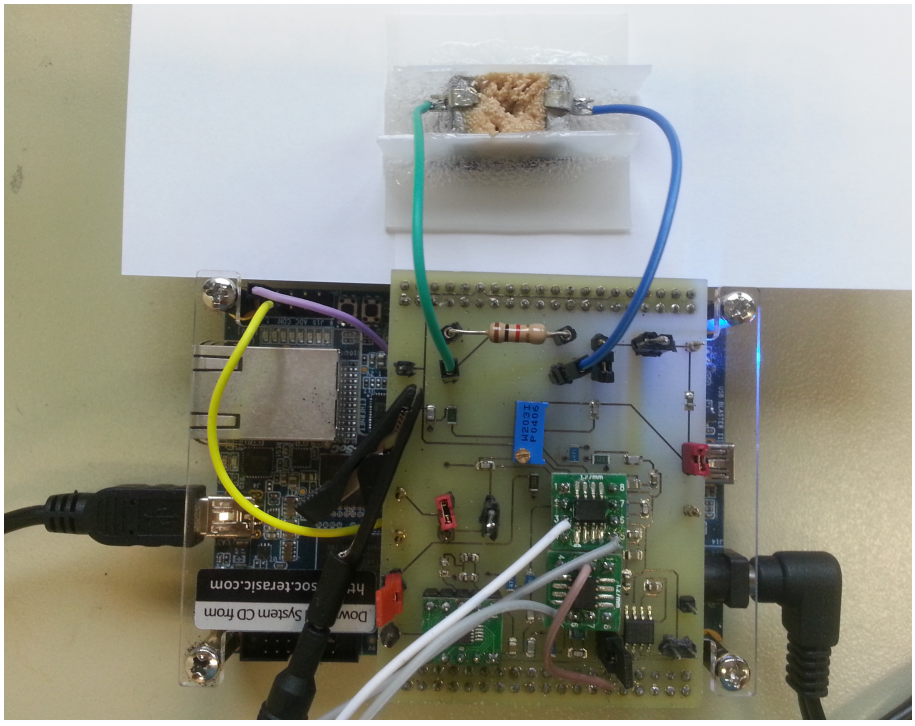

Figure 5.8: Stimulation and impedance measurement of yeast cultures.

The yeast culture were deposit in a silicon chamber with two steel electrodes separated by a distance of 1 cm, it was used 50 g of yeast mixed with 0.5 ml of water. The applied voltage had a magnitude of 100 mVpp at 40 kHz, this signal were applied over 30 minutes, and each sample was taken every second. The results obtained with cell stimulator prototype are compared with the ones obtained using the Agilent 4284A LCR meter. Figure 5.9 shows the changes of magnitude and phase

of the yeast culture over time. The results obtained using the cell stimulator were processed using a third-order median filter for removing peaks and decreasing noise.

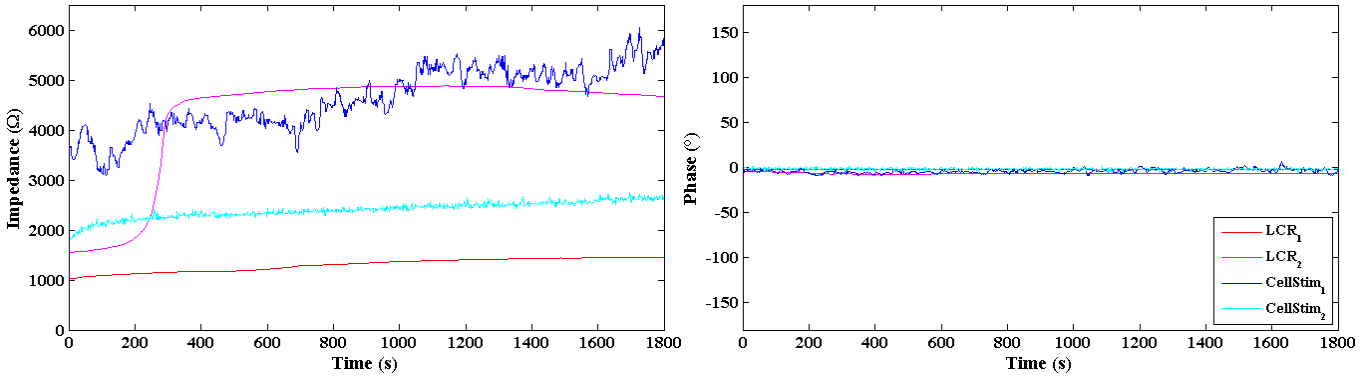

Figure 5.9: Stimulation of yeast cultures at 40 kHz.

The label LCR identify the red and magenta results, these were obtained using the Agilent 4284A LCR meter, and the label CellStim identify the blue and cyan, the ones obtained with the cell stimulator prototype. It can be observed that the impedance magnitude differs from one experiment to another. Even when the same device is used, differences up to 5 kΩ appear. This issue is caused mainly for three reasons: The cell cultures are very sensitive to changes in the environment, and it is not possible to have the exactly same conditions in each experiment. The mixture of yeast and water was not equivalent, shaking a sample in different proportions in each experiment can generates different growth rates. Even most important, the deposition of water in the yeast produces bubbles inside the chamber, causing changes in the electrical permittivity and therefore in the impedance.

Additional error sources affects the results obtained with the cell stimulator due to the circuit is not optimized for noise reduction. Electromagnetic signals in the environment captured by the test pins and jumpers of the PCB, biasing issues from the OA, and quantization error are some of the error sources that introduce noise to the signal.

5.3.3 Stimulating with a frequency sweep

For determining the operation of the device over the bandwidth, frequency sweeps were applied to three different metal film resistors, 3 kΩ, 27 kΩ, and 680 kΩ. The signal applied were a sine-wave with magnitude of 100 mVpp at frequencies up to 125 kHz. The data were processed using a third-order median filter in Matlab software, and the results are showed in Figure 5.10. The red line represents the theoretical value given by the manufacturer, and the blue line represents the results obtained using the cell stimulator prototype.

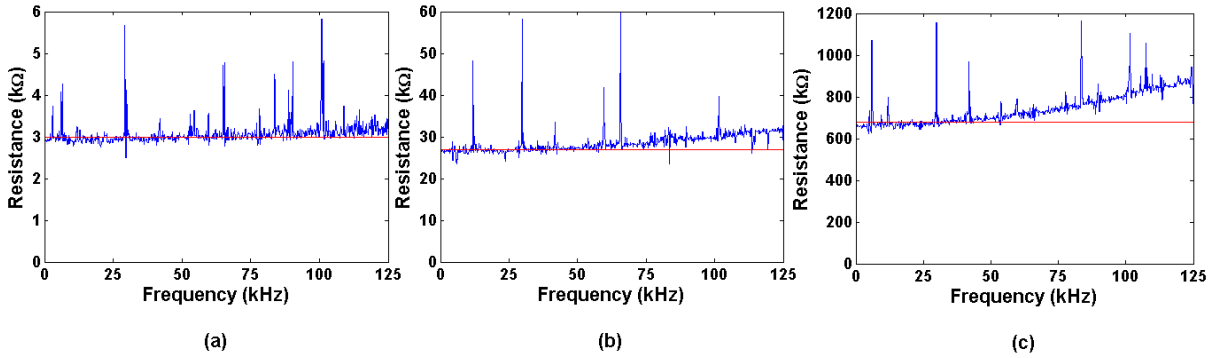

Figure 5.10: Stimulation of known impedance by frequency sweep.

Although the original data were filtered, some peaks remain in the curves since the filter order is not enough to remove them. Tests over the ADC were carried out in order to determine its accuracy, known voltages were applied at the input of the ADC and the digital values were read to estimate the error, variation up to 4 mV were noticed in the conversion. This mean that a critical case in which both, input and output voltages, are affected by this phenomenon there is a difference of 8 mV between signals, this can lead to an error of up to 8.3% in the calculations. Also, it is possible to observe that the system has more difficulty calculating the impedance at high frequencies, especially at high impedances. When high impedance is measured, it is necessary to use high feedback resistors in the I2V, this resistor modify the filter response, the cut-off frequency decreases as the feedback resistors increments. It cause the attenuation of the signals at high frequencies. Table 5.4 shows the average resistance computed using measures up to 40 kHz and 125 kHz.

Table 5.4: Calculations of resistance over a frequency range.

	Up to 40 kHz		**Up to 125 kHz**	
Theoretical Resistance (Ω)	**Measured Resistance** (Ω)	**% Error**	**Measured Resistance** (Ω)	**% Error**
3000.00	2983.20	0.56	3076.67	2.56
27000.00	27003.18	0.01	28603.59	5.94
680000.00	678967.19	0.15	744839.05	9.54

The error percentages presented in table 5.4 shows that the average error remains under 1% for frequency sweeps up to 40 kHz, but for higher frequencies it increases. However it remains below 10%.

Chapter 6

Conclusions

This thesis has presented the design and implementation of a prototype for stimulation and impedance measurement of cell samples. The device had an implementation cost of €160, which is 30 times less than a commercial LCR meter, its dimensions are 75x100x50 mm, which make it suitable for portability (this characteristics are explained with more detail in Appendix D). Also, it establishes the basis for developing others devices with improvements in bandwidth, impedance range and number of channels. In the next paragraphs, the achievements and limitations of this work are presented.

It was shown that the stimulation is achieve by generating sine, triangular and square signals at frequencies up to 1 MHz and magnitudes up to 100 mVpp. The applied signal can be configured as single frequency or as a frequency sweep. Tests carried out with the device showed that magnitudes up to 1 MΩ can be measured with error percentages below 10$\%$ for frequencies up to 40 kHz, and below 15$\%$ for frequencies up to 100 kHz. Also, impedance phase can be measured with error percentages below 10$\%$ for frequencies up to 100 kHz.

The experiments carried out on yeast cell cultures showed large differences between the measurements even when the same device were used, the impedance changed from one experiment to another. Differences in the environmental conditions and the formation of bubbles inside the chamber were random issues that made difficult to reproduce the results.

Finally, for future work, some recommendations can be followed in order to improve the range of measurements as well as the quality of the results. One comprises the use of external ADCs for reducing the phase shift error, since the voltages are sampled at the same time, and improving resolution and bandwidth, it can be achieved if the ADC is selected with more bits and a higher sample ratio. It is important to consider that for incrementing the bandwidth, it can be necessary to implement the FFT inside the FPGA instead of implementing it by software. This would increase the system speed allowing to operate the system at higher frequencies.

Improvements on the analog frontend imply to incorporate voltage followers at the input of the filters for preventing changes in the filter response, it will allow to increase the impedance range. In general, the bandwidth can be improved with faster devices for wave generation, filtering and conditioning. The detectable impedance range can also be expanded by increasing the number of bits of the sampling devices. Finally, the input channels can be multiplexed in a future design for parallel experiments.

A last recommendation is to implement a systematize methodology for validation of the system. It must consider the changes in the impedance even when the preparation of the cultures is similar. It can be achieved by alternately measuring the same sample with the LCR meter and the cell stimulator prototype in short time periods.

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Appendix A

Generated signals for electric stimulation

Figure A.1 is an example of a sine signal in three different frequency levels, Figure A.2 shows the results for a triangular signal, and Figure A.3 for a square signal.

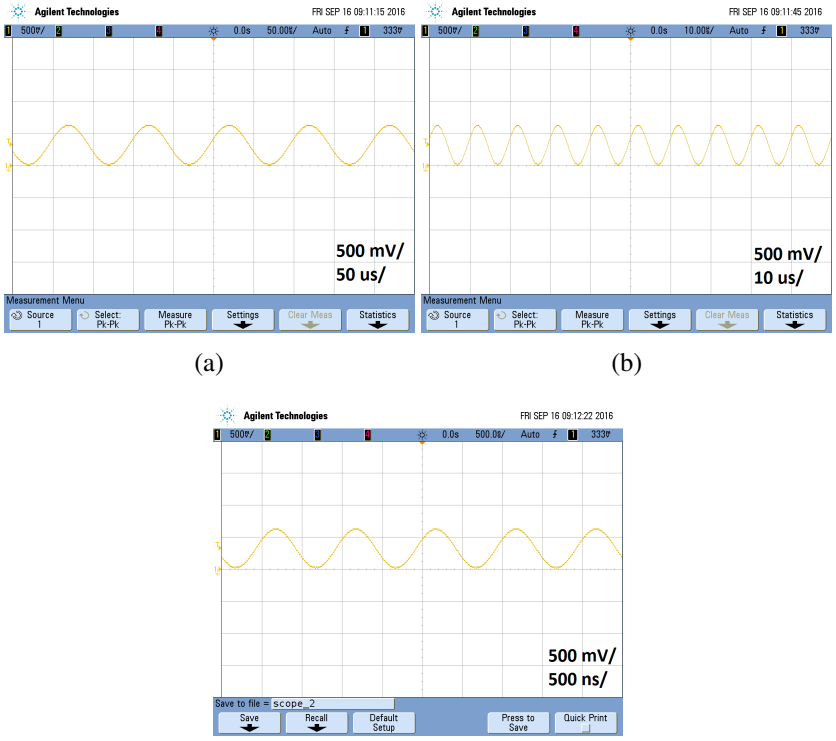
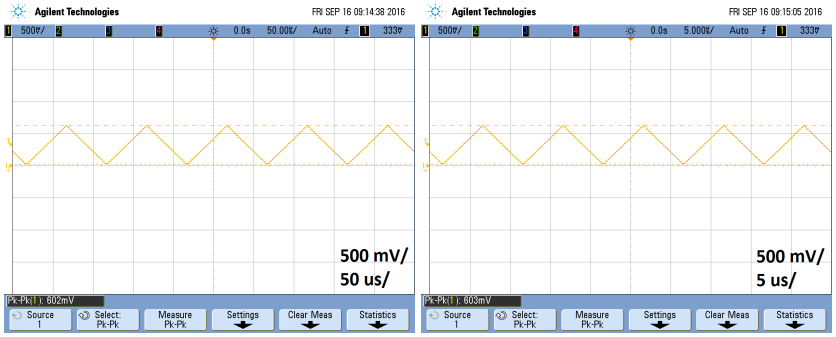
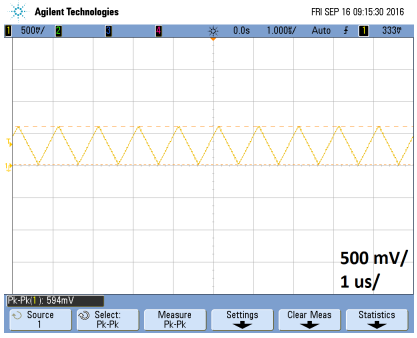


Figure A.1: Sine waveform generation at (a) 10 kHz, (b) 100 kHz and (c) 1 MHz.



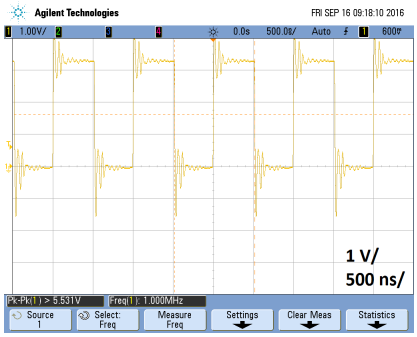
(a) (b)



(c)

Figure A.2: Triangular waveform generation at (a) 10 kHz, (b) 100 kHz and (c) 1 MHz.

(a) (b)



(c)

Figure A.3: Square waveform generation at (a) 10 kHz, (b) 100 kHz and (c) 1 MHz.

Appendix B

Designed software

This appendix shows the code programmed in Python to execute the user interface, impedance calculation and storage, as well as the code used to program the FPGA using Verilog language.

B.1 Python script

This code is executed on the Linux image loaded to the HPS of the DE0-Nano-SoC development board. It is intended to map the registers addresses to a user space in order to establish communication between the HPS and the FPGA, display the user interface, configure the stimulation parameters, perform the FFT, calculate the impedance, and store the data.

```
import os
import mmap
import time
from struct import unpack
import numpy as np
import matplotlib.pyplot as plt

print('*************************************************\n')
print('*    Low-frequency cell stimulator      *\n')
print('*************************************************\n\n')
print('Exit with control+C')
# Run by writting in the console the following command:
# apt-get install python-numpy python-matplotlib
# python2.7 Cell_Stim.py

# Definitions from hps.h
ALT_STM_OFST =     np.uint32(0xfc000000)
ALT_LWFPGASLVS_OFST = np.uint32(0xff200000)

# Definitions from Qsys from hps_0.h
AVALON_INTERFACE_MEMR_0_BASE =  np.uint32(0x00)
AVALON_INTERFACE_MEMR_0_SPAN =  32
AVALON_INTERFACE_MEMR_0_END = np.uint32(0x0f)
ADC_0_BASE =  np.uint32(0x20)
ADC_0_SPAN =  32
ADC_0_END = np.uint32(0x3f)
```

```
# Definitions for this file
HW_REGS_BASE = ALT_STM_OFST
HW_REGS_SPAN = np.uint32(0x04000000)
HW_REGS_MASK = np.uint32(HW_REGS_SPAN-1)

#//////////////////////////////////////////////////////////////////
#//           Map Adress
#//////////////////////////////////////////////////////////////////

# Map the address space for the registers into user space, so we can interact with them.

# Open the memory space (mmap)
fd = os.open("/dev/mem", os.O_RDWR | os.O_SYNC)
vbase = mmap.mmap(fd, HW_REGS_SPAN, mmap.MAP_SHARED, (mmap.PROT_WRITE | mmap.PROT_READ), access=mmap
    .ACCESS_WRITE, offset=HW_REGS_BASE) #Device base address, given by Qsys

# Calculate physical addresses for peripherals
reg_addr = (np.uint32(ALT_LWFPGASLVS_OFST + AVALON_INTERFACE_MEMR_0_BASE) & np.uint32(HW_REGS_MASK))
ADC_addr = (np.uint32(ALT_LWFPGASLVS_OFST + ADC_0_BASE) & np.uint32(HW_REGS_MASK))

#//////////////////////////////////////////////////////////////////
#//          Defined Functions
#//////////////////////////////////////////////////////////////////

# Define DDS write funtion

def dds_write(pwf, pfq, ppshift, preg_addr):

# Set configure register high to prepare serial communication with DDS
vbase.seek(preg_addr+10)                # Place the cursor at configuration register position
vbase.write(np.uint16(0xFFFF))              # Write configuration register

time.sleep(0.001)

# Select the values of the Control and Exit Register according with the waveform selected
if (pwf == 1):
pctrl = 0x2100
pext  = 0x2000
if(pwf == 2):
pctrl = 0x2102
pext  = 0x2002
if (pwf == 3):
pctrl = 0x2128
pext  = 0x2028

freq = np.uint32((pfq*268.435456)/25)
plsb = (np.uint32(0x3FFF) & freq) | 0x4000        #LSB Frequency Register
pmsb = (freq >> 14) | 0x4000                #MSB Frequency Register

ppshift = (ppshift*4096)/360
ppreg = 0xC000 | ppshift                      #Phase Register

vbase.seek(preg_addr)                   # Place the cursor at control register position
vbase.write(np.uint16(pctrl))             # Write control register
vbase.seek(preg_addr+2)                   # Place the cursor at LSB register position
vbase.write(np.uint16(plsb))              # Write LSB register
vbase.seek(preg_addr+4)                 # Place the cursor at MSB register position
vbase.write(np.uint16(pmsb))              # Write MSB register
```

```
vbase.seek(preg_addr+6)                    # Place the cursor at phase register position
vbase.write(np.uint16(ppreg))              # Write phase register
vbase.seek(preg_addr+8)                    # Place the cursor at exit register position
vbase.write(np.uint16(pext))               # Write exit register

vbase.seek(preg_addr+10)                 # Place the cursor at configure register position
vbase.write(np.uint16(0x0000))               # Write configure register

#End function

# Define FFT funtion

def fastft(pstart_time, pADC_addr, pfbkr):

# Read 1024 samples and store them in memory
N = 1024                           # number of samples
ADC1 = [None]*N                        # Preallocate lists with 1024 "None"
ADC0 = [None]*N
index = [None]*N
for c in range(0,N):
vbase.seek(pADC_addr)                      # place the cursor at CH0 position
vbase.write(chr(0x0000))                     # start ADC conversion
vbase.seek(pADC_addr)                  # look CH0
ADC0[c] = list(unpack('I',vbase.read(4)))[0]      # Read channel 0
vbase.seek(pADC_addr + 4)                # look CH1 (ch 1 x 4 = 4)
ADC1[c] = list(unpack('I',vbase.read(4)))[0]      # Read channel 1
#print('ADC0: ',ADC0[c], 'ADC1: ', ADC1[c])

# Calculate the FFT and convert array to list
ftADC0 = list(np.fft.fft(ADC0))              # performs FFT with numpy library
ftADC1 = list(np.fft.fft(ADC1))
# Scale the FFT by dividing by N
for c in range(0,N):
ftADC0[c] = ftADC0[c]/N
ftADC1[c] = ftADC1[c]/N
# Detecting peaks of the FFT
dcvalues = [ftADC0[0],ftADC1[0]]               # Store the DC values
print('dcvalues: ',ftADC0[0],ftADC1[0])
del ftADC0[0]                        # Remove the DC value
del ftADC1[0]                        # Remove the DC value
# Find max value and index for ADC0 (vi)
maxv0 = ftADC0[0]
maxix = 1                            # initial value in case there is no max
for i in range(0,N-1):                     # (1024 values (0 to 1023))
if (ftADC0[i] > maxv0):
maxv0 = ftADC0[i]
maxix = i
# Evaluate ADC1 (vo) in this index
maxv1 = ftADC1[maxix];
# Calculating the impedance
imp = pfbkr * maxv0 / maxv1
magn = abs(imp)
ph  = phase(imp)
exectime = (time.time()-start_time)
print('Magnitude: ',magn, 'Phase: ',ph, 'Time: ', exectime)
print('max0',abs(maxv0), 'max1',abs(maxv1), 'Rfbk', pfbkr)
# Save impedance to a file
myFile = open('impedance.txt','a')               # open a file for appending
myFile.write(str(exectime)+' '+str(imp)+'\n')
```

```
myFile.close()
# Save magnitude to a file
myFile = open('magnitude.txt','a')              # open a file for appending
myFile.write(str(exectime)+' '+str(magn)+'\n')
myFile.close()
# Save phase to a file
myFile = open('phase.txt','a')              # open a file for appending
myFile.write(str(exectime)+' '+str(ph)+'\n')
myFile.close()

return (exectime, imp)

#End function

#////////////////////////////////////////////////////////////////
#//       Programming DDS Registers
#////////////////////////////////////////////////////////////////

print('*************************************************\n\n')

print('Enter the value in Ohm of the feedback resistor:\n')
try:
fbkr=int(raw_input('Resistor:'))
except ValueError:
print ('Not a number')

print('*************************************************\n\n')

print('Select an operation mode:\n')
print('1. Single frequency\n')
print('2. Frequency sweep\n')
try:
mod=int(raw_input('Mode:'))
except ValueError:
print ('Not a number')

print('*************************************************\n\n')

print('Select the waveform:\n')
print('1. Sinusoidal\n')
print('2. Triangular\n')
print('3. Square\n\n')
try:
wf=int(raw_input('Wafeform:'))
except ValueError:
print ('Not a number')

if (mod == 1):
print('*************************************************\n\n')
print('Enter the value of frequency in Hz:\n\n')
try:
fq=int(raw_input('Frequency:'))
except ValueError:
print ('Not a number')

print('*************************************************\n\n')
print('Enter the phase shift in degrees (from 0 to 359 degrees):\n\n')
try:
pshift=int(raw_input('Phase shift:'))
```

```
except ValueError:
print ('Not a number')

dds_write(wf, fq, pshift, reg_addr)

# Set a timer for program execution
start_time = time.time()

while 1:
(exctmp, mimp) = fastft(start_time, ADC_addr, fbkr)

else:
pshift = 0
B = 1250          #125
FQ = [None]*B
Tmp = [None]*B
Imp = [None]*B
#Beging a new reading
myFile = open('impedance.txt','a')              # open a file for appending
myFile.write('Feedback Resistor:'+str(fbkr)+'\n')
myFile.close()
myFile = open('magnitude.txt','a')              # open a file for appending
myFile.write('Feedback Resistor:'+str(fbkr)+'\n')
myFile.close()
myFile = open('phase.txt','a')              # open a file for appending
myFile.write('Feedback Resistor:'+str(fbkr)+'\n')
myFile.close()
# Set a timer for program execution
start_time = time.time()
for j in range(1,B):
fq = 100*j
dds_write(wf, fq, pshift, reg_addr)
(exctmp, mimp) = fastft(start_time, ADC_addr, fbkr)
FQ[j] = fq
Tmp[j] = exctmp
Imp[j] = abs(mimp)
print('Impedance:', Imp[j], 'Freq:', fq)

# Plot the magnitude
plt.figure(1,figsize=(4,3),dpi=90)  # figure of 4x3 inches at 90 dpi
plt.plot(FQ, abs(Imp))
plt.xlabel('Frequency',fontsize=14)
plt.ylabel('Magnitude',fontsize=14)
plt.grid(True)
plt.legend()
plt.show()

# Plot the phase
plt.figure(2,figsize=(4,3),dpi=90)  # figure of 4x3 inches at 90 dpi
plt.plot(FQ, phase(Imp))
plt.xlabel('Frequency',fontsize=14)
plt.ylabel('Phase',fontsize=14)
plt.grid(True)
plt.legend()
plt.show()
```

B.2 Verilog code for serial protocol

This code is intended to take the stimulation parameters generated by the preview Python code, and write the internal registers of the Programable Waveform Generator, AD9833, by serial protocol.

```
module serdds (clk50, clk25, start, control, lsbfreq, msbfreq, phase, ext, sdata, fsync, sclk);

input clk50;
input clk25;
input start;

input [15:0] control;              //Control Register
input [15:0] lsbfreq;              //LSB Frequency Register
input [15:0] msbfreq;              //MSB Frequency Register
input [15:0] phase;                //Phase Register
input [15:0] ext;                  //Exit Register

output sdata;                     //Data to be transmited
output fsync;                     //Enables or desables the transmition
output sclk;                      //Protocol Clock


reg        count2;                 //Keeps the sdata bits for two periods of clock
reg [2:0]  count4;                 //Time beetwen transmitions
reg [2:0]  count5;                 //Stores the count of sended registers
reg [3:0]  count15;                //Stores the count of sended sdata bits
reg [79:0] enable;                 //Enables the SCLK during transmitions
reg [15:0] tempdata;                 //Data to be transmitted
reg       temsync;                 //~Fsync


always@(negedge clk50)

begin

if (start)
begin

count2   <= 1'b0;
count4   <= 3'b000;
count5   <= 3'b000;
count15  <= 4'b0000;
tempdata <= 16'h0000;
temsync  <= 1'b0;
enable   <= 80'hFFFFFFFFFFFFFFFFFFFF; // Write 80'b in 1 as enable register

end
else
begin

if(count5 < 3'b101)
begin

if (clk25 && enable[79] && count15==4'b0000 && count2==1'b0)
begin

temsync <= 1;
```

```
case (count5)
3'b000 :                // Control Register
tempdata <= control;

3'b001 :                // LSB Frequency Register
tempdata <= lsbfreq;

3'b010 :                // MSB Frequency Register
tempdata <= msbfreq;

3'b011 :                  // Phase Register
tempdata <= phase;

3'b100 :                  // Exit Register
tempdata <= ext;

endcase

end
else
begin

if (count15 == 4'b1111 && count2 == 1'b1)
begin

temsync <= 0;
if (count4 == 3'b100)
begin

count5  <= count5 + 3'b001;
count2   <= 1'b0;
count4   <= 3'b000;
count15  <= 4'b000;

end
else
begin

count4 <= count4 + 3'b001;

end
end
else
begin
if(temsync == 1)
begin
if (count2 == 1'b1)
begin
tempdata <= tempdata << 1;
enable <= enable << 1;
count15 <= count15 + 16'h0001;
count2 <= 1'b0;
end
else
begin
tempdata <= tempdata;
count2 <= count2 + 1'b1;
end
```

```
end
else
begin
temsync <= temsync;
end
end
end
end
else
begin

temsync <= 1'b0;
enable   <= 80'h00000000000000000000; //Desable SCLK

end
end
end

assign sclk = clk25 && enable[79];
assign fsync = ~temsync;
assign sdata = tempdata[15];

endmodule
```

Appendix C

PCB design

C.1 First prototype

Figure C.1 shows the schematic for the first design. This design include many test pins and stage jumpers for internal analysis of the device.

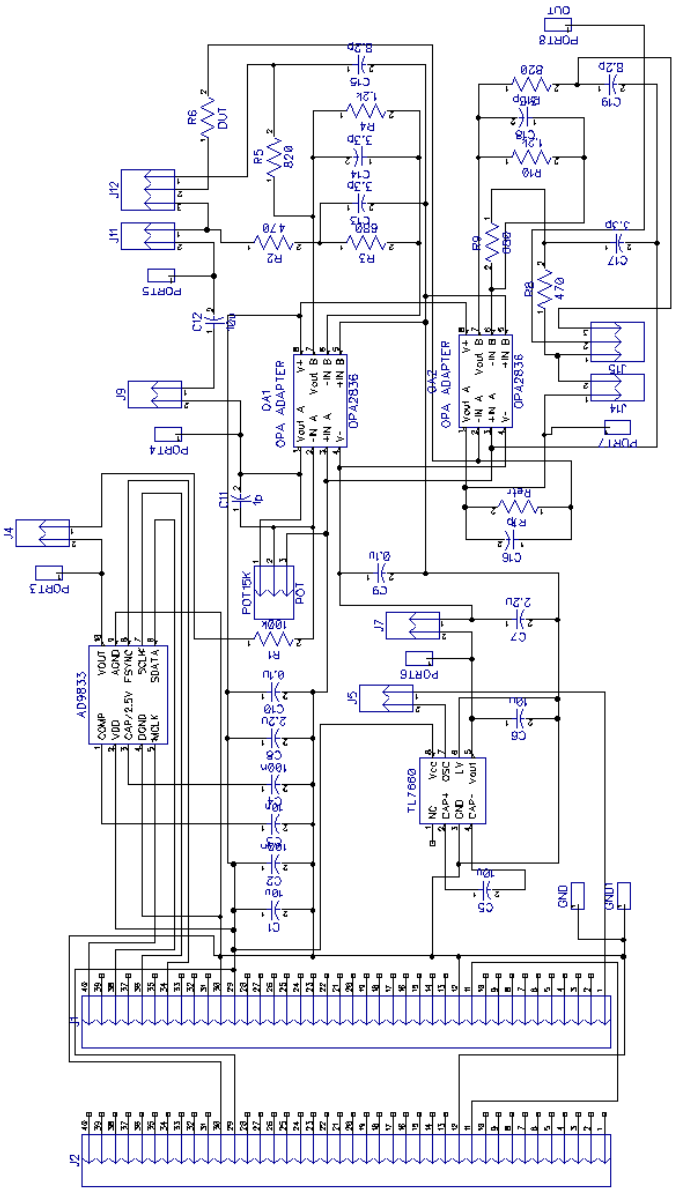


Figure C.1: Electric diagram of the first prototype.

Figure C.2 shows the PCB layout for the first implementation.

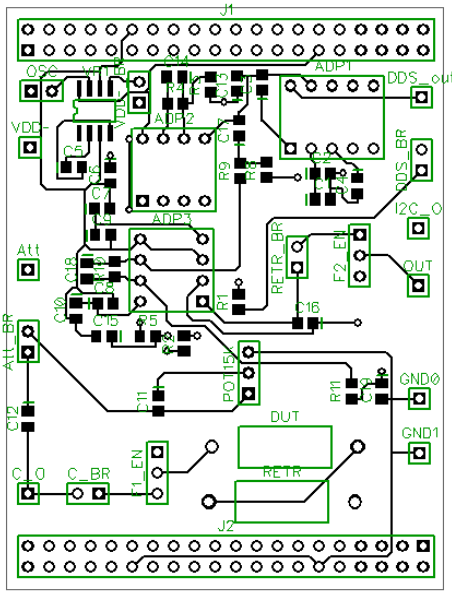


Figure C.2: PCB design of the first prototype.

C.2 Second prototype

A second device was design to incorporate external ADCs with faster sampling rates for achieving a higher bandwidth, this design eliminates the test pins and stage jumpers included in the first device. However, due to time constraints and delays in the fabrication of the PCB the system was not tested.

The AD9225 is an ADC that accomplish the circuit requirements, it has 12 bits of resolution, sample ratio of 25 MSPS and SHA at the input, allowing voltage resolution below 1 mV and input signal frequencies above 125 kHz. Figure C.3 shows its electric diagram, the external circuitry configures the IC for accept signals with ground reference in a range of 2 Vpp.

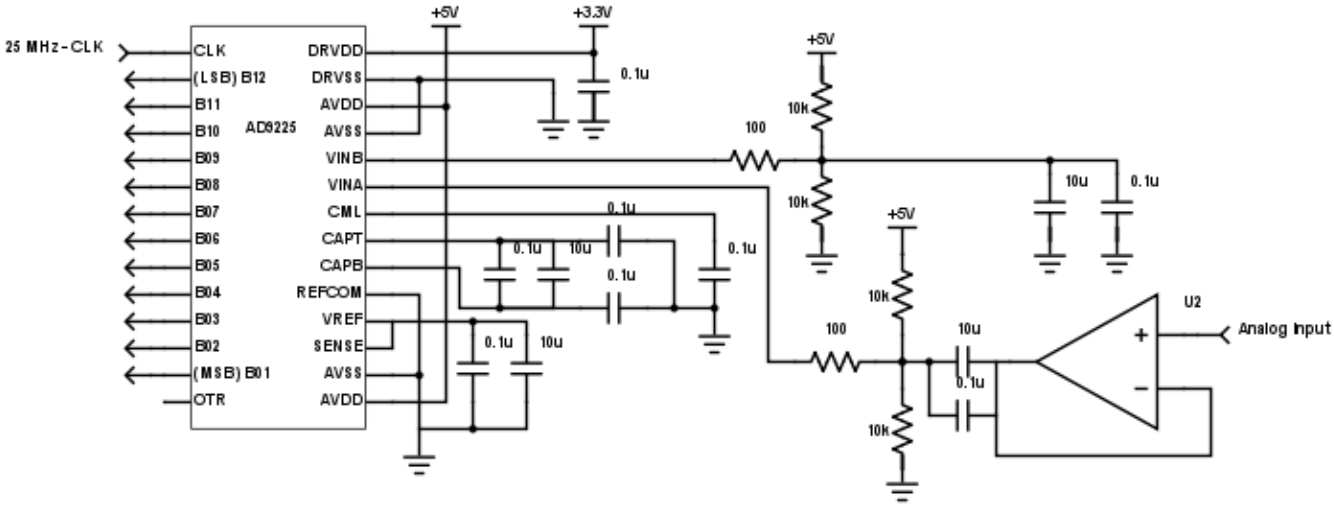


Figure C.3: Electric diagram of the ADC

Sub-systems for signal generation and data acquisition are the same as the designed in the first prototype. Figure C.4 shows the schematic for the second design.

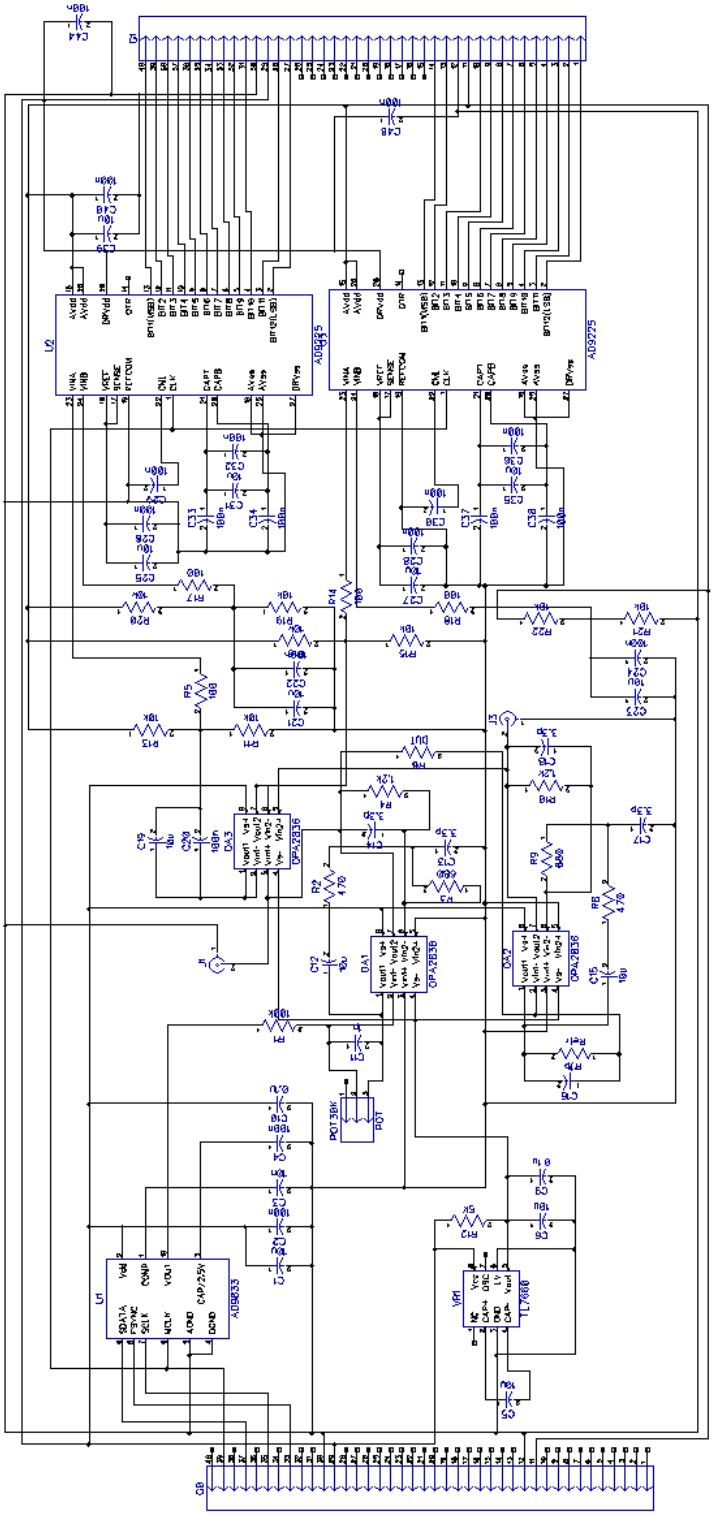


Figure C.4: Electric diagram of the second prototype.

Figure C.5 shows the PCB layout for the second implementation.

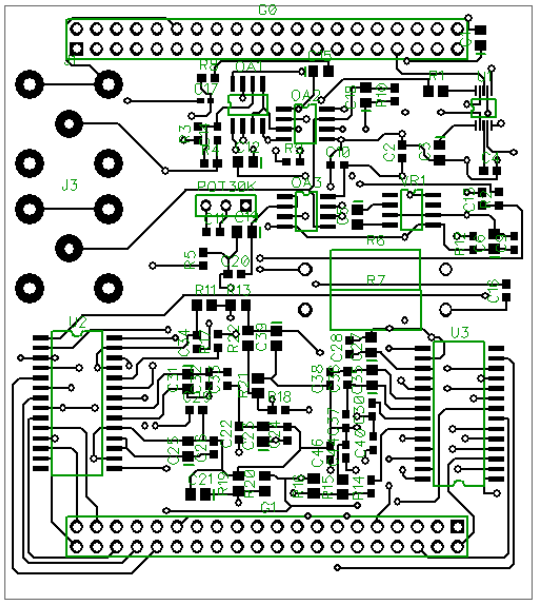


Figure C.5: PCB design of the second prototype.

Appendix D

Cost and size characteristics

The cost by components, as well as the total cost of the designed device is showed in Table D.1.

Table D.1: Manufacturing cost.

Component	**Quantity**	**Price (€)**
DE0-Nano-Soc	1	91
OPA2836	2	7.12
TL7660	1	1.19
AD9833	1	8.34
Capacitors	19	0.2882
Resistor	11	0.1669
Variable resistor	1	2.28
PCB	1	50
Total		**160.38**

Finally the device dimensions are: 10x7x5 cm.