Instituto Tecnológico de Costa Rica

Escuela de Ingeniería Electrónica

Characterization and Validation of Interconnect Models for a PCIExpress Bus

Graduation Project report to qualify for the title of Electronics Engineer with the Licentiate's degree

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Cartago, Costa Rica

June 19, 2018

Instituto Tecnológico de Costa Rica
Escuela de Ingeniería en Electrónica
Graduation Project
Evaluation Board

Graduation project presented as a requirement to opt for the title of Electronics Engineering with the academic degree of Licentiate in Electronics Engineering, of the Instituto Tecnológico de Costa Rica.

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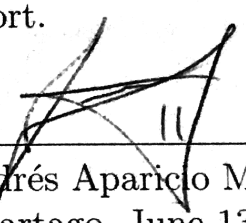

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Cartago, June 13, 2018
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Abstract

In this work a segmented approach to model a PCI Express PCB-buses channel is analyzed. The channel models are built with a 3D full-wave approach in order to compare the results obtained from 2D and 3D simulations, with segmented models that were previously available. The goal is to verify the accuracy of the segmented models and methodologies, in order to assess if a segmented methodology would still be feasible for the next generations systems (e.g. PCIe 5.0). In the development of this work the construction process and necessary simulations to analyze the data transmission are shown, considering the motherboard transition from the via array supporting the package to the PCIe interface connector. Models of vias and transmission lines are developed in order to characterize the PCIe buses.

Keywords: DC-Blocking Capacitors, Differential Signaling, Interconnects, PCIExpress, S Parameters, Signal Integrity.

Resumen

En este trabajo se analiza un enfoque segmentado para modelar un canal de buses PCB PCI Express. Los modelos de canal se construyen con una aproximación de onda completa 3D para comparar los resultados obtenidos de las simulaciones 2D y 3D, con los modelos segmentados que estaban previamente disponibles. El objetivo es verificar la precisión de los modelos y metodologías segmentadas, con el fin de evaluar si una metodología segmentada todavía sería factible para los sistemas de próxima generación (por ejemplo, PCIe 5.0). En el desarrollo de este trabajo, el proceso de construcción y simulaciones necesarias para analizar la transmisión de datos se mostrarán, teniendo en cuenta la transición de la placa madre desde el arreglo de vías que soporta el paquete hasta el conector de interfaz PCIe. Se desarrollarán modelos de vías y líneas de transmisión para caracterizar los buses PCIe.

Palabras clave: Capacitores de Bloqueo CD, Interconexiones, Integridad de Señal, Parámetros S, PCIExpress, Señales Diferenciales.

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First of all I want to thank God for allowing me to be with health, wisdom and understanding until the final stage of my career at TEC. I know that without Him I could not have overcome all the obstacles and challenges that came before me to be where I am now.

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Javier Aparicio Morales

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1 Introduction

The Instituto Tecnológico de Costa Rica works on research projects in the field of signal integrity, which consists of the study of the electrical problems that arise in high speed digital designs and the possible solutions to them. This field of interest also belongs to Intel, where they also seek to analyze and verify the transmission of data at high speeds. With the same purpose of research held by ITCR and Intel, a joint collaboration will be carried out to analyze and compare the scope of the project with previous research that exists on the subject.

Signal integrity in modern systems is a concern due to the fact these computer systems are currently operating at speeds in the Gb/s range. Therefore, it is important that the performance of data buses can operate at high speeds without loss of information [1]. It is then sought that the channel designs consider a sufficient bandwidth to transmit these volumes of information. The growth of bandwidth, generates problems at the physical level. Signal integrity problems of a channel include the parasitic effects on discontinuities such as connectors, material losses, and electromagnetic coupling.

Problems with the waveform of the signals also occur. The problem is a wave degradation, distortion or alteration of the waveform. It must be considered that being digital circuits, the signals are binary, therefore the effect on these systems is to achieve the interpretation of the logic levels [2]. Other effects related to high data rate generate are reflections, as well as parasitic effects that arise from the materials that make up the communication channel [3].

PCI Express (PCIe) buses use a set of differential pairs to carry very high speed information between the CPU and the device of interest. Some typical uses of PCIe include graphics cards and storage devices. The fourth generation of the standard uses binary signals at 16 Giga-samples/second (GS/s). The fifth generation (in the process of standardization) will be extended to 32 GS/s [4].

The traditional analysis technique for PCIe buses consists of the mathematical concatenation of separate models, corresponding to the main elements that the signal must pass through. These include the packaging, the socket, the buses, the PCB with vertical interconnections (vias), the DC-blocking capacitors and the connector itself. This topology is depicted in figure 1.1.

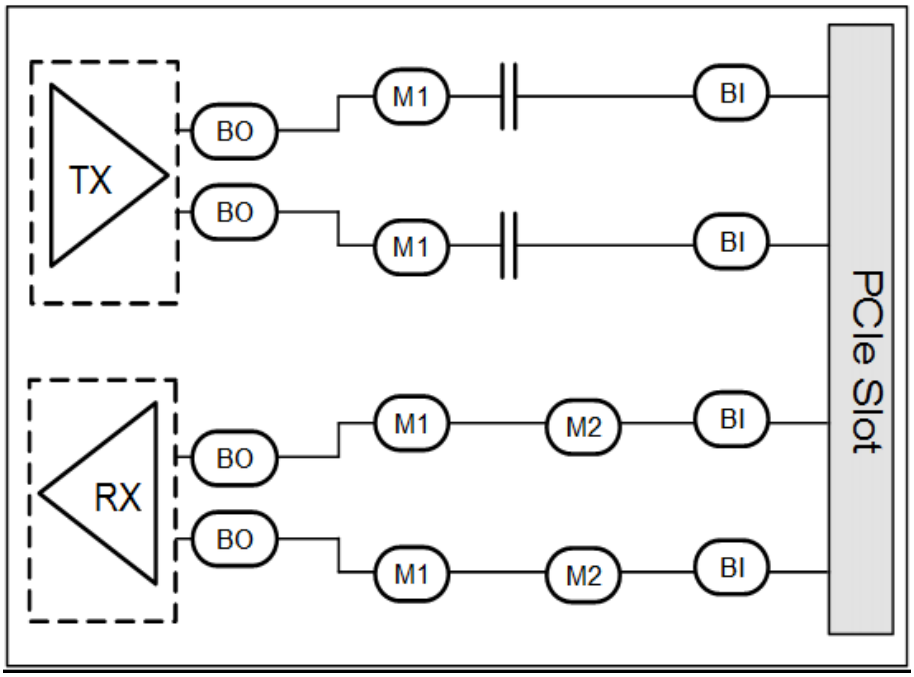


Figure 1.1: Direct topology of a PCIe link [4]

Currently, a segmented methodology for the signal paths is being used. Some models are obtained from wave simulators in two dimensions, some others in three dimensions, and some are obtained from measurement results. The concatenation is carried out through the technique of synthesis of S parameters. Although this methodology has been validated in the past, by means of correlations with real measurements. The speeds of operation have increased very significantly and there is doubt about the validity of the method for higher speeds.

Therefore, it is sought to validate the method by segmentation of a PCIe bus through a three dimensional model of the same topology, where the main characteristics of the signal transmission channel at the simulation level are contemplated. To achieve the characterization of a three dimensional model, it must be taken into account how the model is constituted, this to consider all the dimensions it has, as well as the electrical characteristics it has.

Taking into consideration the technical specifications of the topology, the next step is to construct the 3D models that constitute the PCIExpress bus at PCB level. Both, independent parts of the models and the concatenated signal paths are compared. Other important considerations are the impedances in the differential pairs, the materials by which the components are built, as well the transmission gains and reflection that exist in the channel's discontinuities. Also DC-blocking caps are included, in order to block the DC component of the signal.

The construction of a three dimensional model will allow to determine the most significant

electrical effects that can be observed by the S parameters. Among the effects are the insertion loss, return loss, crosstalk and impedance profile [3]. With the obtained results of the three dimensional model, they will be compared with the results obtained from equivalent models, They are generated by means of synthesis of S parameters of the individual models generated by different methodologies.

This will make it possible to observe differences between both approaches, in order to determine if the use of the segmented models are still valid for the new operating speeds, or if it is necessary to make a change to the three dimensional model since it contemplates more interactions in comparison to the segmented one. It will be shown that similarities, dependences of parameters that must be revised with respect to real platform.

1.1. Objectives

1.1.1. General Objective

Evaluate a methodology for modeling high speed electrical channels in PCIe 4.0 interfaces, based on three dimensional models and full wave simulations.

1.1.2. Specific Objectives

1. Develop the physical channel model based on the specification of a PCIe bus from a personal computer motherboard.
2. Simulate through a wave based approach to complete the channel model, obtaining the microwave parameters as a result of the simulation.
3. Validate the simulated three dimensional model with respect to available alternative simulation methodologies.

1.2. Work organization

This report contains various chapters. *Chapter 2* deals with theoretically base terms such as: transmission lines, parameters obtained from the lines, PCB's (Printed Circuit Board), stackups, vias, materials technology, the PCIe connector and signal and power integrity.

In the *Chapter 3* will describe the steps necessary for the realization of high speed channels, where the corresponding results and analysis will be attached. Everything will be done in three dimensional models using a full-wave approach.

Finally, the *Chapter 4* a correlation will be made between the results obtained from chapter three and the results that Intel has about these channels through segmented methods. This correlation will seek to validate the segmentation of the channels or if it's necessary emigrate to three dimensional models for the development of these channels.

2 Theoretical Foundation

In this section, concepts such as printed circuit boards, how they are made up, materials and components that are included in the printed circuit boards will be addressed. A vital issue in the transmission of high speed signals will be mentioned and this is the signal and power integrity. These envelop a general level analysis in the frequency and time domain. The transmission lines, which are the paths to transmit signals, are essential in high data speed channels and will be also mentioned. Finally, the PCI Express connector will be mentioned. It will be treated how it is constituted, physical and electrical characteristics it has, as well as how the connector works.

2.1. Printed Circuit Boards (PCB's)

The section on printed circuits boards will be developed, where topics such as the types of PCB's, elements containing PCB's and the materials that are usually used in manufacturing processes will be discussed in greater depth.

A PCB (Printed Circuit Board) or PWB (Printed Wire Board) is a mechanism to support and electrical. Perform connections of electronics components through conductive traces, pads and other characteristics recorded in copper sheets on a non-conductive substrate are allowed [5]. Figure 2.1 is observed a four layer PCB with a transversal cut. Besides, there are different types of PCB's in terms of the number of layers or types. In addition, these must be complied with the next characteristics [6]:

- Power source of energy for the other layers.
- Dissipation of energy from its components.
- Serve as support for the components.
- Achieve to interconnect the circuit components with various layers making up the PCB.

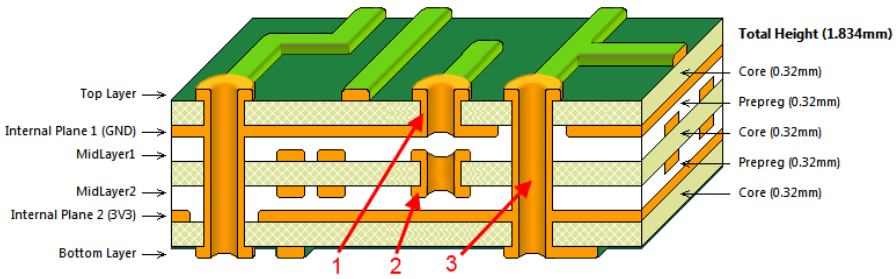


Figure 2.1: Four layer PCB with blind via (1), buried via (2) and through hole via (3). Taken from [6]

2.1.1. PCB Types

As it was mentioned implicitly in the characteristics. A laminated PCB can be of different forms, these are [6]-[7]:

- PCB of one layer: Conductive layer and a dielectric is consisted. This type can contain an upper layer of soldermask and silkscreen. It is used in low cost and high production circuits due to the simplicity with which this type of board is allowed.
- Two layer PCB: Two conductive layers are composed. They can be connected through vias or with the use of surface mount technologies (SMT). The connections are made in the plates at a surface level without the need to use vias [8]. Meaning that these plates use most of the time only one of the conductive layers.
- PCB with more than two layers: In more complex designs are used when a greater number of interconnections are used. Also to avoid unwanted effects such as heat or electromagnetic phenomena.
- Flexible PCB: Flexible and non-rigid materials are used. The great advantage is that can be used on surfaces that are bent. In addition to reducing the cost and weight compared to a rigid plate.

2.1.2. Vias and Their Effects

As shown in figure 2.1, there are different types of vias that to the main traces of the conductive layers are connected. These routes according to the signal topology and the reference levels that are part of the transition are classified. A type is the through hole via, which all the layers of the PCB pass through. There is the blind via that crosses only a section of the layers and it is visible only by one of the outer layers of the PCB. Finally, there is the buried via that is internally and it is not visible in any of the outer layers of the PCB [9].

Effects in the signals transmission of the common or differential lines are produced by signal vias. The most loss are generated by these vias because field lines are created by the antipads around the vias and an increase in capacitive coupling is generated. This is represented as an additional discontinuity in signal propagation [10].

The signal vias with antipads are used, as the reference and power planes from the main signal can be isolated. There are different structures such as rectangular, circular, oval. Structures that use oval antipads are the ones that have the lowest reflection. Figure 2.2 is depicted an example of vias in a PCB, where the reference vias, antipads, and the signal vias are included [11].

Another type of via is the return via. In greater quantity to reduce the crosstalk effects they are used, which between the signal vias and the reference planes are originated. The signal to noise ratio is maintained by this via. A portion of the currents of the vias flow over the reference planes are allowed. These vias nearby to the signal vias must be, to eliminate unwanted effects, which in the parallel plates are originated [9]-[12].

A cross-section of a signal via is depicted in figure 2.3. It can be seen that the signal travels in this via and with a stripline is connected . A return current will travel back to the via input (upper side of the figure), through the power or reference vias if exist on the PCB. If these vias do not exist, the current will return as a displacement current between the reference planes. Signal losses and interactions with other PCB elements are generated by this displacement. At the level of electric fields around the vias, modes on the parallel plates are generated, which results in a loss of power and reduction of signal strength. Finally, the highest impedance coupling between the vias and the traces to avoid reflections that result in power losses must be presented. A considerable number of return vias allow the signal loss to be reduced considerably [13].

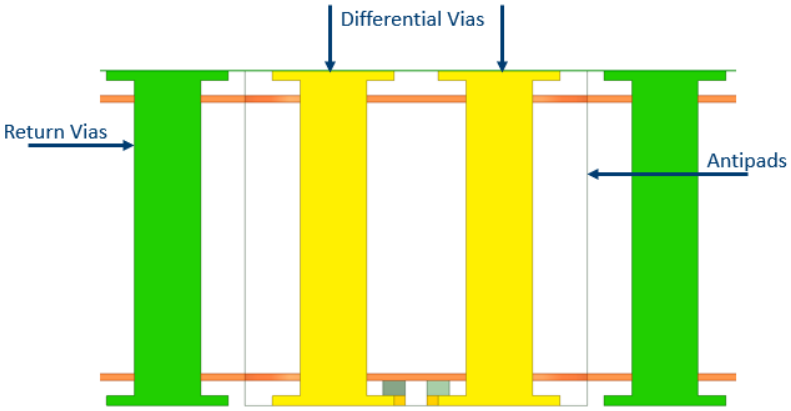


Figure 2.2: Types of Vias in a Multilayer PCB. Taken from [11]

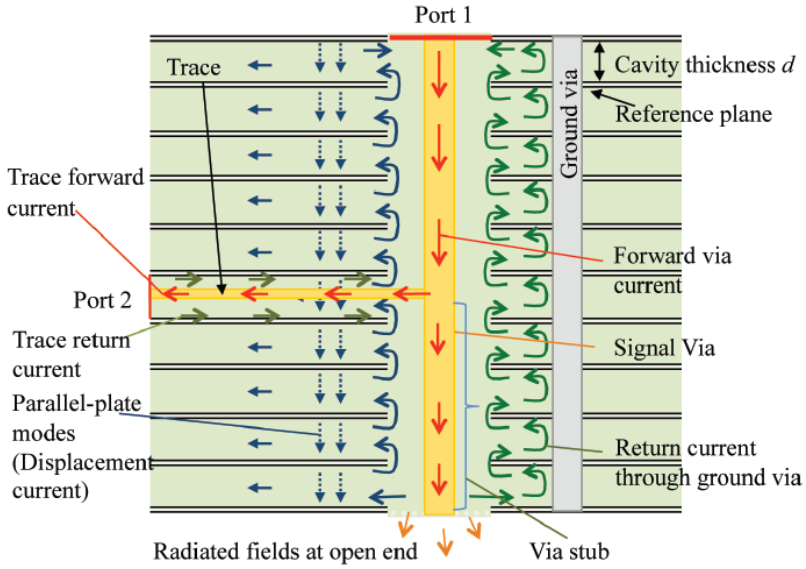


Figure 2.3: Cross-section of a signal and ground via in a multilayered PCB. Taken from [13]

Copper in a PCB is used. For the conductive traces, the power, and reference planes are used. Other layers such as dielectrics, use a material called prepreg. It is a fiber sheet impregnated with resin, which allows pressure and heat to join stacked cores. The core is another cured dielectric bonded together by two metal plates. Another material that can be used as a dielectric is FR4. The arrangement of these layers together with the conductors is called *stackup* [9]-[14].

The traces on the superficial layers, as well as the internal, must have symmetry and not have angles of 90° in the traces. This not to generate effects such as interference and discontinuities through the line. On the other hand, when it is necessary to make capacitor connections at surface level in the traces. It is recommended not to use a large number of them due discontinuities and increase the losses in high frequency by to parasitic effects can be generated [15]-[16]. Figure 2.4 and 2.5 are shown how the symmetry of the traces should be when using differential channels. In addition to how the capacitors should be connected to the surface level with the traces of the outer layers of the PCB [17].

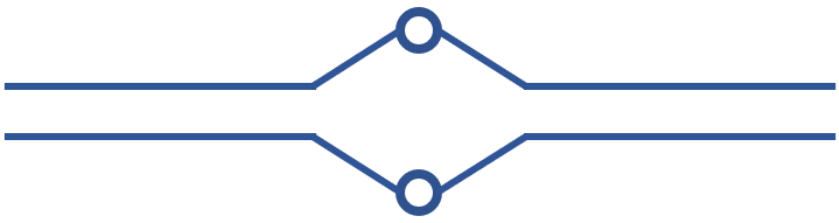


Figure 2.4: Symmetry of differential lines using vias. Own creation

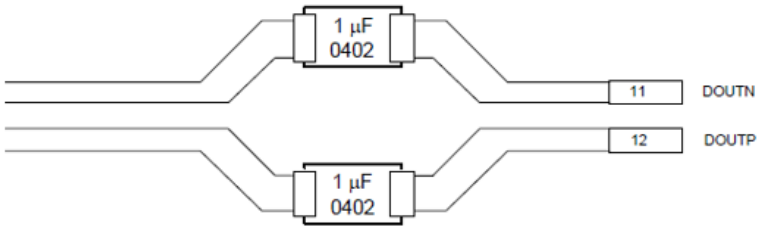


Figure 2.5: Connection of the capacitors at surface level. Taken from [17]

2.2. Signal and Power Integrity

Currently, computer systems demand high rates of data transmission, which implies that must be operated at high frequencies, in the order of GHz. This implies that there are signal integrity problems as well as power problems in the channels. In this section will talk about what should be considered when performing high speed analysis.

2.2.1. Signal Integrity

It is the analysis, design, and validation of the interconnections, in order to guarantee the transmission of the signal, avoiding reflections and losses to the maximum [18]. The analysis in time and frequency domain is related. For example in the frequency domain can be analyzed by S parameters and in the time domain is used an analysis called time domain reflectometry (TDR).

The analysis in the frequency domain normally are related with the utilization of microwave network parameters called S parameters. These parameters represent an equivalent circuit of elements as impedances, inductors, and capacitors. The S Parameters have N-ports input and M-ports of exit. Due that in high frequency is worked, it is necessary to establish resistive terminals in the ports that won't be used at the moment of the measure in order to prevent reflections or interference. The S parameters with forward and backward traveling waves on a transmission line are related, also with the power flow [19].

Measures as reflection coefficient or transmission coefficient indicate how much of the power is reflected and transmitted respectively. Figure 2.6 is depicted the propagation of waves through a line up to a load. The incident wave and reflected wave are observed that by the reflection and transmission coefficients are represented [19]. In general, these parameters in a matrix are represented, where the size of it, depends on the number of ports that device under test (DUT) has.

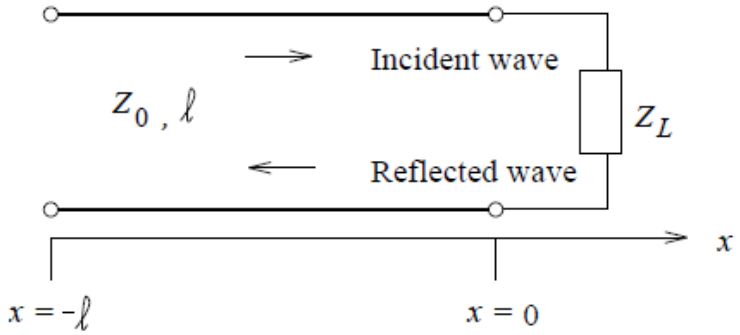


Figure 2.6: Waves propagation through the line up to a load. Taken from [19]

A N-port network is a generalization of the DUT, where in figure 2.7 is shown the general example and as was told, can be a matrix of NxN size as [19]:

$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & \dots & S_{1N} \\ S_{21} & S_{22} & S_{23} & \dots & S_{2N} \\ S_{31} & S_{32} & S_{33} & \dots & S_{3N} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ S_{N1} & S_{N2} & S_{N3} & \dots & S_{NN} \end{bmatrix}$$

A parameter S_{ij} is a measure of a specific input and exit port, where port j is the transmission of the incident wave and port i is the reflected wave. The coefficients can be defined as:

- S_{ii}: reflection coefficient seen looking port i
- S_{ij}: transmission coefficient from j to i

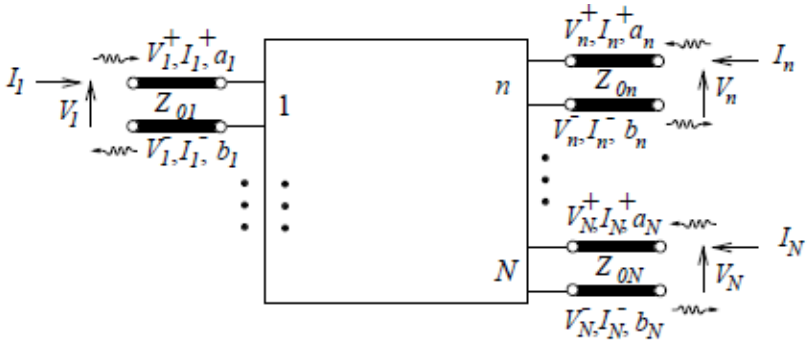


Figure 2.7: N-port network with traveling waves. Taken from [19]

If the DUT has 4 single ports or more, making a conversion to mixed mode is allowed. This mode is a combination of the single ports and if is only used the single mode, it does not provide much insight information about the common and differential mode about the reflection and transmission. The mixed mode is used to know about the differential and common behavior. For the conversion to the mixed mode a four port example will be used but in general, is described as [20]:

$$[S^{mm}] = [M][S][M]^{-1} \tag{1}$$

$$\text{where } [\mathrm{S}^{mm}] = \begin{bmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{bmatrix},$$

$$[\mathrm{S}] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{33} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \text{ and } [\mathrm{M}] = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & -1 \\ 0 & 0 & 1 & 1 \end{bmatrix}$$

A signal along the line in an electromagnetic waveform is propagated. Between two or more conductors are established. When existing more than a conductor line and they are nearby between each other, the electric and magnetic fields of the signal will interact with adjacent conductors. A coupling of energy from one line to other is induced when a stimulus is applied and is called *crosstalk*. For example in digital systems many lines in parallel through packages are routed. Connectors, PCB's and the crosstalk is important to contemplate it. Signal integrity by the crosstalk is affected. The characteristic impedance and propagation velocity are modified. Also the noise margins are reduced [2].

For crosstalk, the mutual inductance and capacitance by coupled of multiple conductors due to the magnetic field (mutual inductance) and electric field (mutual capacitance) are caused. Mutual inductance L_M induces a current from a driven line onto a quiet line by means of the magnetic field. While the mutual capacitance C_M is the coupling of conductors by the electric field [2]. Figure 2.8 is observed the principle of mutual inductance and capacitive are[2].

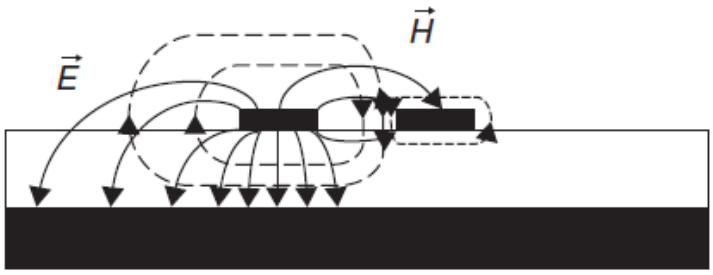


Figure 2.8: General idea of mutual inductance and mutual capacitance. Taken from [2]

Finally, crosstalk either at the beginning of the stimulus or the end of the line can be measured, in other words, the load. The first method is called NEXT and with the coupled of energy at the beginning of two nearby lines are related. The second is the FEXT and between the source and the final of the next line is measured, in figure 2.9 is observed how the crosstalk has to be measured [21].

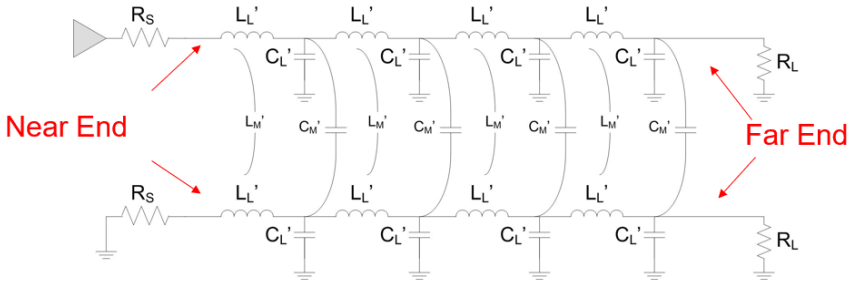


Figure 2.9: NEXT and FEXT in two transmission lines. Taken from [21]

Another requirement in RF circuits is the use of lumped elements for many purposes like matching networks, lossless DC connection, harmonic tuning and to ensure stability at frequencies below the cutoff frequency [19]. The primary lumped elements on RF circuits are resistors, capacitors, and inductors. In PCIe channels, the used of capacitors are necessary to block the DC component. Figure 2.10 shows different lumped capacitors, and for this lumped element exists different types such as [19]:

- Metal-dielectric-metal capacitor: using the interconnect metalization.
- Metal-dielectric-semiconductor capacitor: it's used in MOS transistor.
- Semiconductor junction capacitor: Either the capacitance of *pn* junction or Schottky barrier.

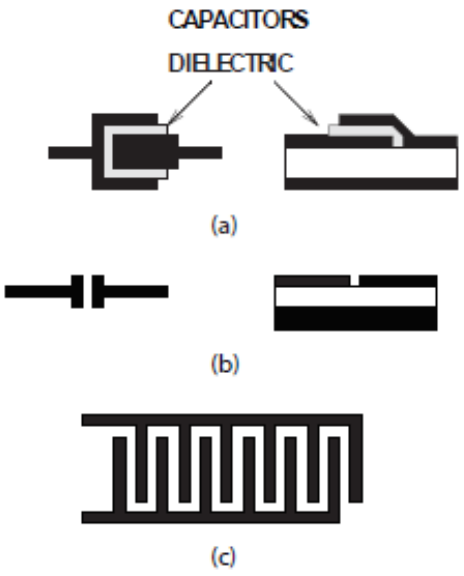


Figure 2.10: Capacitor elements: (a) parallel plate capacitor; (b) gap capacitor; and (c) interdigitated capacitor. Taken from [19]

For the analysis of the transmissions lines, time domain analysis is another possibility to see the transmission of the signals. The matching of the line with a stimulus and see the response through the time can be observed. A common test pattern in time domain is a PRBS (Pseudo Random Binary Sequence), which can emulate the random nature of binary coded information. To see this behavior, an eye diagram is used. All the bits into a short interval are folded in this diagram and an accumulation of distorted edges and levels voltages are displayed [22].

An example of this diagram is observed in figure 2.11 where four bits are observed in the diagram. It can be seen the opening of the eye indicates that it is possible to differentiate between a "high" and "low" level. . This opening to the level voltage of the bit is related and depends on the system in which voltage as a high level or low level is taken. Another fact that can be studied from the diagram is the time transition of the bits. Different times of the bit transitions produce an issue called jitter and this is the difference between all the transitions of the bits. A good jitter is when the changes occur approximately at the same time. The distortion of the transmission happens for the mismatch of the impedance, noise and, demand of a system. Beyond of frequency of operation will cause a closing of the eye, which also would increases the jitter [22].

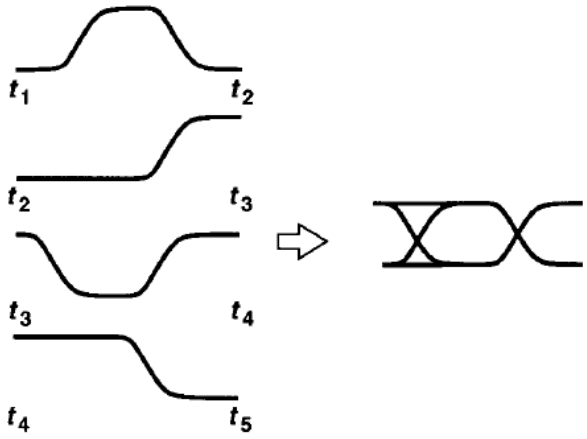


Figure 2.11: Response of a sequence of bits. Taken from [22]

A technique is used in time domain analysis is the Time Domain Reflectometry (TDR). This technique use the premise of multiple reflections derive an impedance profile of the DUT. To make this measure a diagram like in figure 2.12 is used. A step function is used that is the stimulus and is driven to the DUT through a 50 Ω cable. With an oscilloscope the waveform at A is observed, which represents the voltage profile of the reflected waves. This voltage to an impedance profile is converted, which to measure the characteristic impedance and propagation delay of the line can be used. By the waveform of the impedance profile, a DUT can have inductive or capacitive behavior and also see exactly, where the discontinuity is due to the elements of the system [2]. A response of the TDR in terms of inductive and capacitive behavior is observed in figure 2.13, where a decrease of the plot is a capacitive trend and when increased is an inductive trend [23].

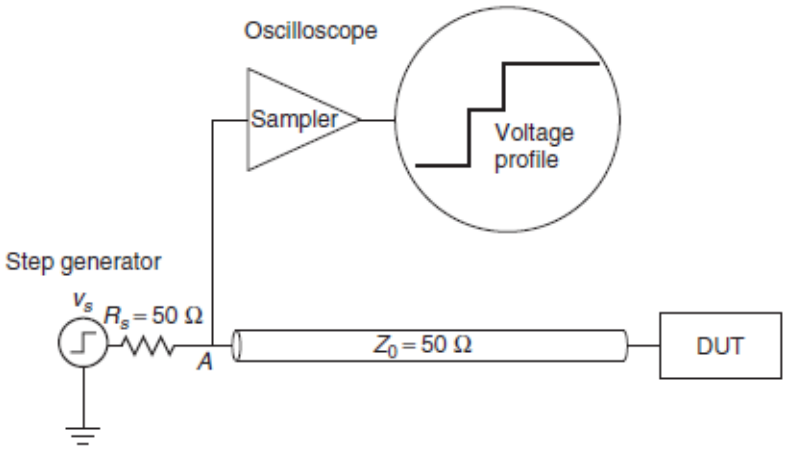


Figure 2.12: Generic TDR measurement setup. Taken from [2]

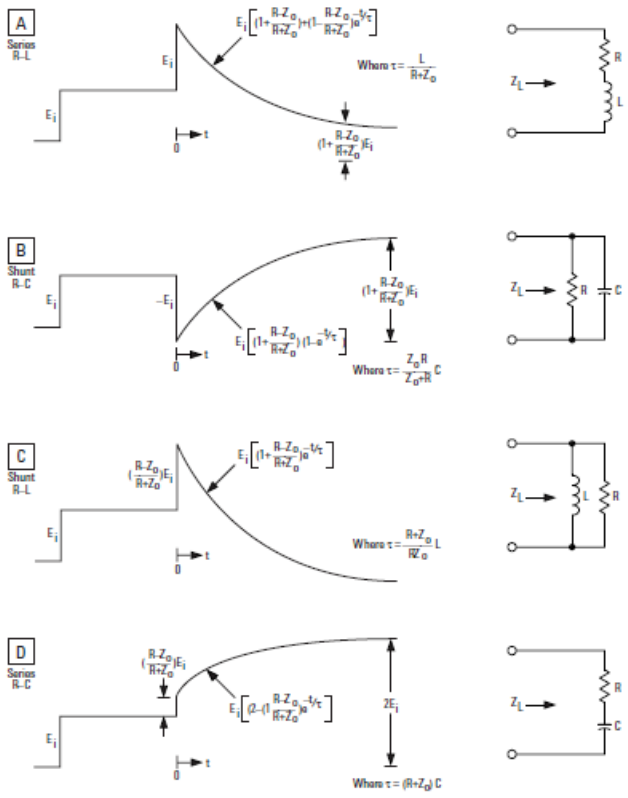


Figure 2.13: Response of the DUT in terms of capacitive and inductive behavior. Taken from [23]

2.2.2. Power Integrity

Responsible to analyze and design the network source of the system, starting with coupling, assignment planes and stackup. An important element for the analysis of the power integrity is the PDN (Power Delivery Network) which candles for a stable source voltage [18]-[24]. For a good analysis of the PDN, several elements must be analyzed and these are:

- DC Resistance: By the geometry of the net is determined, also is a conductor material. To reduce the resistance is preferable to use wide traces and avoid discontinuities.
- Capacitor Loop Inductance: By this parameter, the effectiveness of a decoupling capacitor is quantified. To achieve the decoupling, the reference and power planes should be near to the top and bottom layers. Use capacitors near of this planes to avoid discontinuities are recommended.
- Target Impedance: To calculate the impedance of all power network is used, starting from S parameters and TDR analysis are calculated.

All the elements of the PDN can be depicted in figure 2.14. The DC resistance is showed caused by the source voltage. Decoupling in various ways either using DC-blocking caps

or power and reference planes can be given. Finally, all the network must have a target impedance that is the operation value for the system works well [25]. Table 2.1 is showed the issues either for signal integrity or power integrity that have been discussed previously.

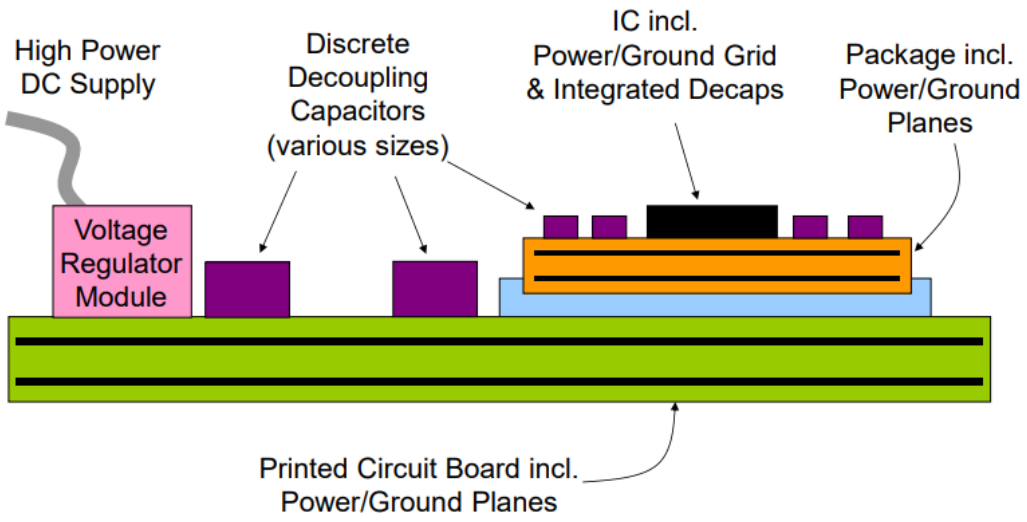


Figure 2.14: Basic PDN Elements. Taken from [25]

Table 2.1: Summary of the issues of Signal Power Integrity

Element	**Issues**
Signal Integrity	Attenuation, Reflection, Dispersion, Interference and Crosstalk
Power Integrity	Voltage Drop, Noise and Crosstalk

2.3. Transmission Lines

As mentioned, the fundamental part in the transmission of electrical signals are the medium by which are transmitted, for instance, in the transmission of signals between the motherboard, interfaces, and peripherals. The transmission lines are the most used because operate in the speed ranges in which this work is being developed.

The transmission lines to transmit electrical energy and signals from one point to another are used, from a source to some load [26]. These from two or more parallel conductors are composed that connect the source with the load. There are different types of lines, which can be observed in figure 2.15. Between the types are the coaxial cables, the microstrip lines, and striplines. The lines can be differential and common. For the design of PCB's in high frequency microstrips are used due they are the most common [27]-[28].

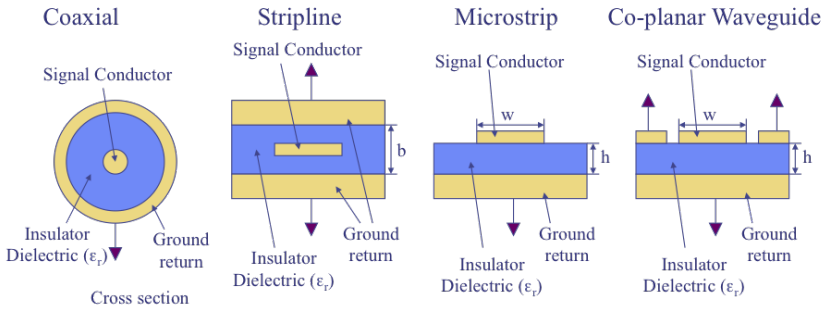


Figure 2.15: Transmission lines types. Taken from [28]

A transmission line from their lumped elements can be modeled using a differential line segment and their associated lumped elements per unit length. These elements are resistances (R), inductors (L), conductances (G) and capacitors (C), and a combination of all are known as *RLGC* matrix. A representation of this, is observed in figure 2.16. The equations to model the transmission line with RLGC elements are [29]-[30]-[31]:

$$\frac{\partial \mathbf{v}(x,\omega)}{\partial x} = (\mathbf{R}(\omega) + \mathbf{j}\omega\mathbf{L}(\omega))\mathbf{i}(x,\omega) \tag{2}$$

$$\frac{\partial \mathbf{i}(x,\omega)}{\partial x} = (\mathbf{G}(\omega) + \mathbf{j}\omega\mathbf{C}(\omega))\mathbf{v}(x,\omega) \tag{3}$$

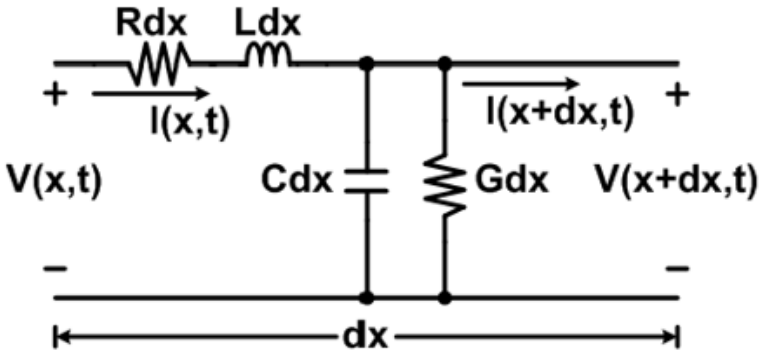


Figure 2.16: RLGC model of a transmission line. Taken from [30]

With the equations 2 and 3 the propagation constant γ and the impedance *Zo* of the line can be obtained . These equations are described as [29]:

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{4}$$

$$Zo = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}} \tag{5}$$

2.3.1. Microstrip Lines

The microstrip lines are the most popular lines because by a photolithographic process are manufactured. In addition are easy to minimize and integrate passive and active microwave devices. The conductive plane that is the main trace has a width W and a reference plane. Both by a dielectric of thickness d and a relative permittivity ϵ_{r} are separated. The description of the microstrip is depicted in figure 2.17 as well as a sketch of the field lines [32].

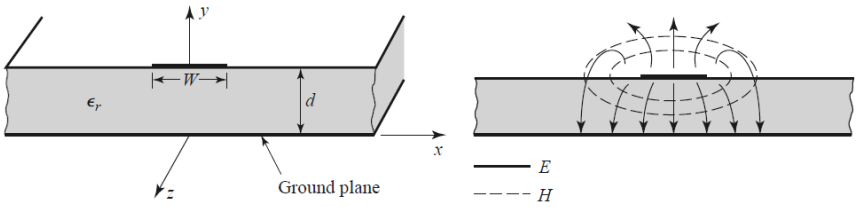


Figure 2.17: Microstrip transmission line. Taken from [32]

2.3.2. Differential Transmission Lines

These type of lines consist of two conductive traces separated by a specific space with a common reference plane. These are used to cancel the effects generated by transmitting a single signal on a single line. Therefore with a differential mode, there are a positive signal and another negative. This configuration causes the effects of the fields to be eliminated and thus avoid degradation of the signals [33]. This topology is depicted in figure 2.18.

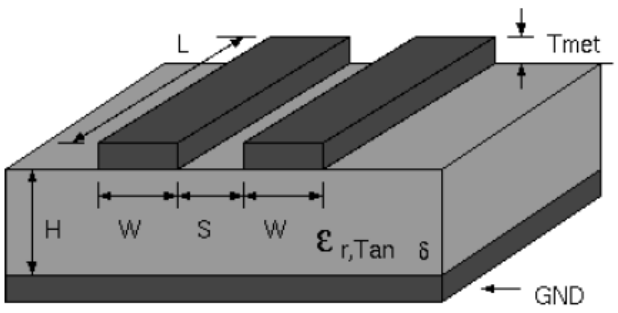


Figure 2.18: Differential Transmission Line. Taken from [33]

As mentioned, using a differential mode helps to avoid signal degradation, but more specifically help to [34]:

1. Reduction of collapse in the lines.
2. Reduction of electromagnetic interference.
3. Improvement in noise immunity.
4. Less sensitivity to attenuation.

A correct differential pair occurs when uniformity in the cross sections, symmetry in the width of the line and the spacing of the dielectric is presented. Finally, there must be a coupling of the source, the line, and the load. The first parameter to approximate in a differential line is the impedance of this, and the following equation is used [35]:

$$Z_{\mathrm{d}} = \frac{174}{\sqrt{\epsilon_{\mathrm{r}} + 1.41}} \ln \frac{5.98h}{0.8w + t}(1 - 0.48e^{-0.96\frac{d}{h}}) \tag{6}$$

Where:

- ϵ_{r} is the relative permittivity of the dielectric.
- h is the thickness of the dielectric.
- w is the width of the trace.
- t is the thickness of the trace.

As the lines are not ideal, these will have losses. They can be represented as reflections in the line discontinuities. To represent the losses, the coefficients of reflection and transmission are used. These coefficients indicate how much of the power and transmitted through the medium is reflected [27]. These are parameters that manage to describe the behavior of a transmission line.

Other losses that are generated in the transmission lines are [2]-[36]-[37]:

- The effect of the dielectric produces that the waves transmission is being in function of the frequency. Since the fundamental frequency, the transmitted power will be minimum. Besides it gets complicated when the dielectric isn't homogeneous because will present more discontinuities than usually.
- DC loss is found and depends on the resistivity of the conductor in a total area in which the current is flowing. This loss can be represented as:

$$R = \frac{L\rho}{Wt} \tag{7}$$

Where L is the length of the line, ρ is the resistivity of the conductor material, W and t are the width and the thickness of the line respectively.

- The skin effect is other loss and is a physical phenomenon related to high frequency transmission on a wire. The electromagnetic field of the wire causes most of the electrical current to become crowded at the edges of the wire. Thus causes that effective resistance of the cable is changed and the current through the wire flows in the skin of the conductor. An increased signal attenuation at higher frequencies is produced. Also can be called as skin depth and can be represent as:

$$\sigma = \sqrt{\frac{\rho}{f\mu\pi}} \tag{8}$$

  Where ρ is the resistivity of the metal, f is the frequency and μ is the permeability of free space.

2.4. PCIExpress

This section contains the basic features of the interface that is used in this work which is the PCI Express. How this connector is constituted, the velocities that can manage and some considerations to built the channel will be shown. It's important to remember that not only is the PCIe connector but also there are buses from a motherboard to the connector. Hence, all these details in sought to get the best transmission of the signals must be considered.

This interface is a bus or network of communications of high speed in short lengths and with low latency for the interconnection of devices and card among themselves inside a chassis. Among the main features that this interface has are [38]:

1. The network by full duplex point to point links is built. Each link by lanes is composed, where each lane is full duplex and consists of two pairs of threads, a pair of transmission and another of reception. The voltage transmitted is differential, which helps to the noise immunity. A diagram of the link is shown in figure 2.19.
2. The transmission is serial, it means that in each lane the transmission of bits in both directions is serial to avoid problems of jitter in the receiver.
3. The bus speed is scalable by adding more lanes to the link where it can be scaled by 1 (x1), 2 (x2), 4 (x4), 8 (x8), 16 (x16) and 32 (x32) lanes per link. Depending on the number of lanes the data transmission is given.
4. Possibility of changing and connecting hot cards, especially in servers.

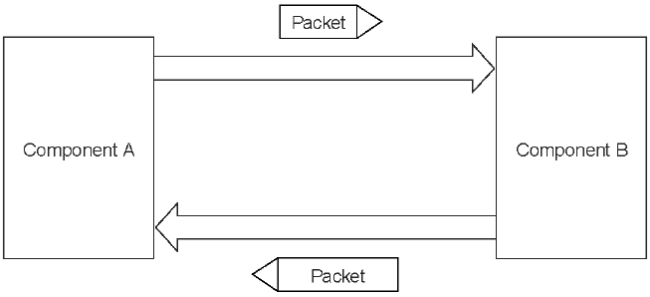


Figure 2.19: Basic link of the PCIe interface point to point. Taken from [38]

Currently, with the PCIe 4.0 is managed to reach speeds up to 16 GB/s per lane. This evolution in the speed of the connector is shown in figure 2.20 [39]. As described in chapter one, a typical PCB link used with this interface is modeled. It contains the breakout in the channel and the characteristics that the breakout must have are [4]:

- The maximum length of seven inches is allowed if is greater than seven then, loss of information will exist.
- The length of each channel must be the same in each lane and must be connected with as few layers as possible.
- The insertion loss permitted is -4 dB at a frequency of 8 GHz and the return loss lesser than -15 dB at the same frequency as for insertion loss. To achieve this, low loss dielectrics are used.
- The impedance of these channels is 100 Ω in differential mode and 50 Ω in common mode. For greater accuracy, the channel must have a tolerance of ± 20% of the mentioned values.

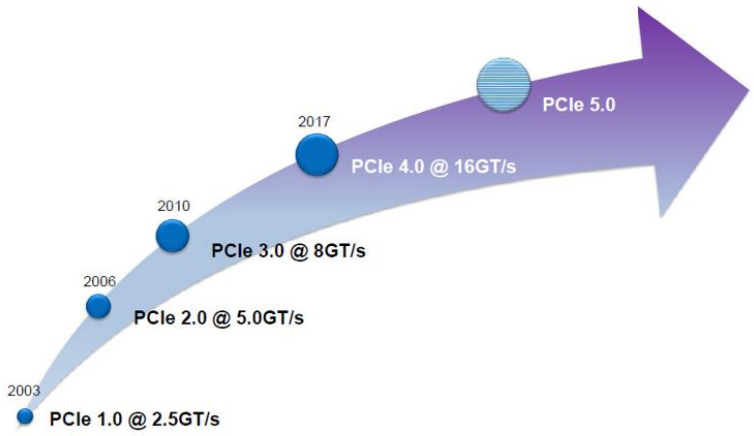


Figure 2.20: Speed evolution of the PCIe connector. Taken from [39]

Given the PCIe operates with differential channels, the interface is managed with differential voltages. A conductor has a negative voltage V_{D-} and another positive V_{D+}. The differential voltage is defined as $V_{DIFF} = V_{D+} - V_{D-}$ and the common mode voltage V_{CM} is obtained from the average of the differential voltages, means $V_{CM} = (V_{D+} + V_{D-})/2$. Figure 2.21 is exemplified the voltage levels of common and differential mode of the breakout, that are connected to the interface PCIe [4]-[40].

The channels used by PCIe require serial capacitors that allow a blocking of the CD component between the reception and transmission stage. The capacitance values used are based on the 0402 standards, which specify the dimensions of the capacitor as length, width and height [41]. The values of capacitance allowed by PCIe 4.0 have a minimum value of 176 to 265 nF as the maximum value [4].

The measurements that the capacitor has, they are given by the 0402 standard which is a SMT assembly. In figure 2.22, the guide to build the capacitor is shown, where the letters represent measures that are shown in the table 2.2 [41].

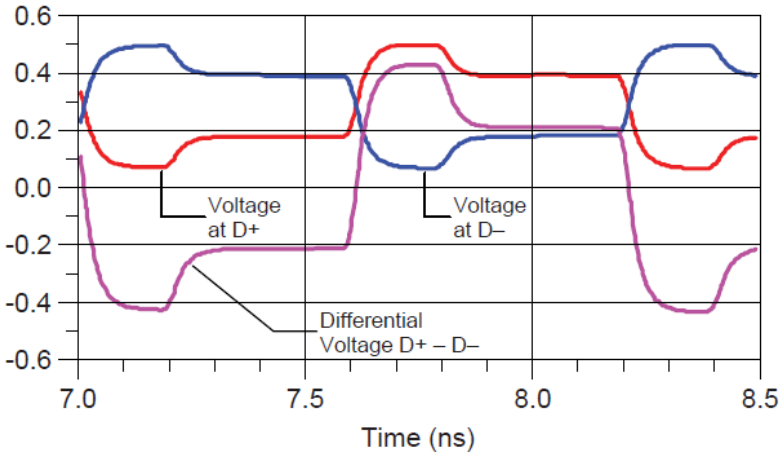


Figure 2.21: Common and differential mode voltage of PCIe connector. Taken from [40]

Table 2.2: Dimensions of capacitor 0402 standard

Standard	A (mm)	B (mm)	C (mm)	D (mm)	E (mm)	F (mm)	G (mm)
0402	1.50	0.40	0.50	0.50	0.10	1.75	0.95

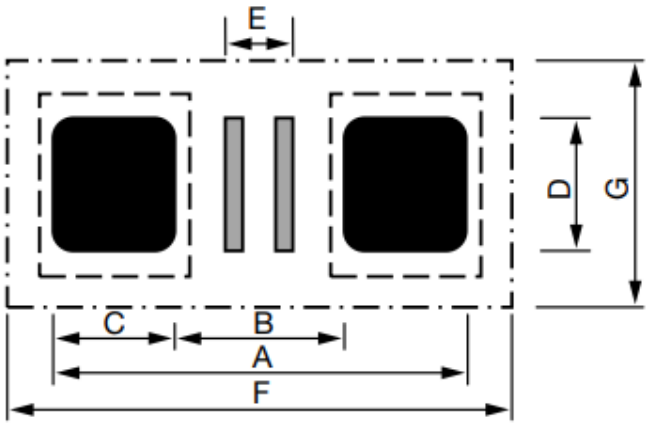


Figure 2.22: Diagram of capacitor under the standard 0402. Taken from [41]

3 Model Generation and Validation

This chapter deals with the modeling of the channel and its building blocks. Each element, has a simulation. The signal integrity and the TDR is analyzed to see the target impedance of the block, in view of complying with the impedance of the system.

3.1. Design Flow

Figure 3.1 is shown the general blocks of the bus. The basic models have to be done first and these are the transmission line, vias, DC-Blocking capacitors and a model of the PCIe connector.

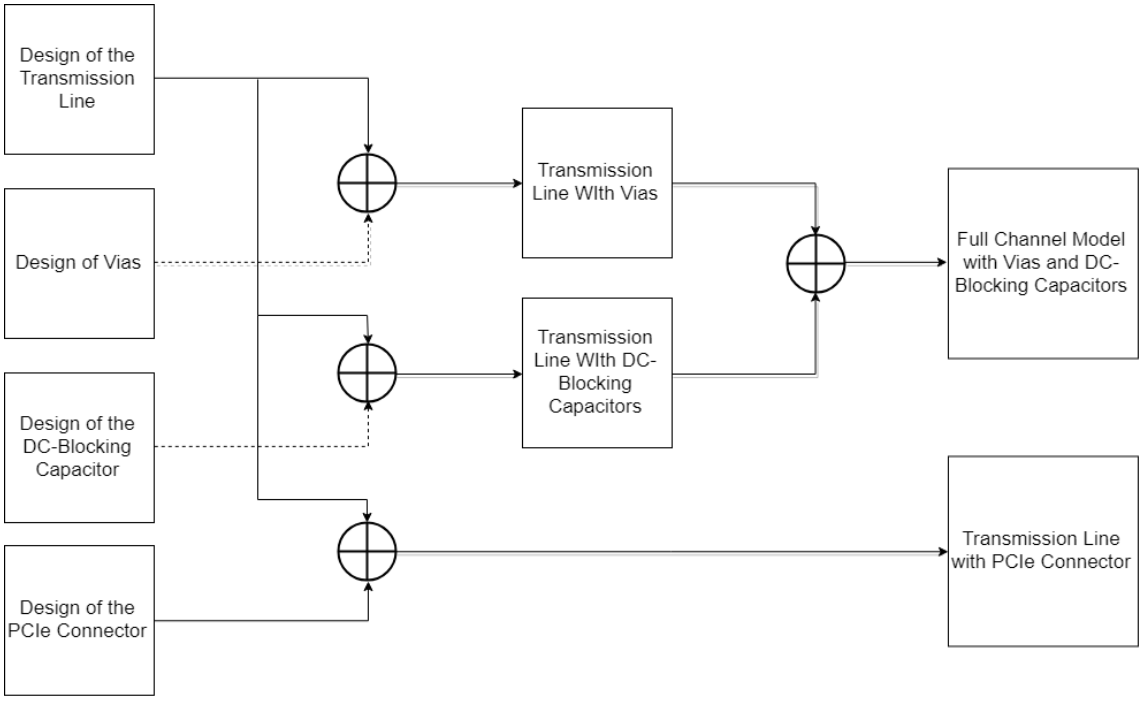


Figure 3.1: General flow design of the 3D PCIe bus

Once the basics models with their respective results are validated. The combined of the basic models must be made. These are three models, which are transmissions lines with vias, transmissions lines with DC-Blocking capacitors and a small card, which is connected to the PCIe connector. Finally, a full channel model with the combined of the capacitors, transmission lines, and vias is built. The goal is to see the response of the channel. The stage between the transmission of a motherboard up to the PCIe connector by the small blocks are conformed.

For the development of the blocks of the figure 3.1, an electromagnetic simulation environment is used. This is Ansys HFSS, it is suitable for high speed designs. In general, to

obtain a result from the simulator, a mesh must be defined. An iterative algorithm solves the fields of the model and refines the mesh until the S parameters converge below a threshold defined by the user. Once the algorithm converged, the solving process is started. The software can use different methods to make the sweep and for this work will be using the *Finite Element Method* (FEM), which handles complex materials and geometries. For the 2D simulations the *Boundary Element Method* (BEM) is used. This approach is a numerical method to resolve equations in partial derivatives linear that have been formulated as integral equations [42].

Another tool that will permit the analysis of the blocks is a mathematical software called Matlab. This will allow to analyze the S Parameters obtained from the HFFS simulator. Measures relate to the transmission and reflection of the signals can be studied. Besides, make transformations from single to differential, as well as to concatenate the S parameters, to make the larger models [43].

3.2. Channel Specifications

The building block models are developed considering a four layer stackup. Some basic models as the transmission lines or the DC-Blocking capacitors can be modeled using only two layers of the four. Table 3.1 show the specifications of the different layers, wherein the case of the microstrip lines are two types that in later subsections will be developed. These specifications are available and also used for the segmented approach.

Table 3.1: Channel Specifications of the four layer stackup

Routing Layer	**Layer Description**	**Tline Type**	**Thickness (mil)**	**Dielectric Constant**	**Loss Tangent**
	Soldermask		0.65	3.4	0.031
1	Breakout (BO), Main Route (MR)	MS	1.9		
	Prepreg		2.75	3.7	0.017
2	Power	PWR	1.1811		
	Core		49.01575	4.125	0.015
3	Ground	GND	1.1811		
	Prepreg		2.75	3.7	0.017
4	Breakout (BO), Main Route (MR)	MS	1.9		
	Soldermask		0.65	3.4	0.031

For the range of frequency that will be covered for all the models, a broadband sweep will be used. This band covers from DC up to 50 GHz, with a step of 0.125 GHz and a total points of the sweep are 400 with an error of the 4%. A TDR analysis will be applied, and the principal feature that this analysis has, its the time rise which is 40 *ps*.

3.3. Transmission Line

In this section the transmission line models will be modeled that PCIe buses use. These are two models, where one is located near to the motherboard and the other is the main route that allows the signal to be carried from the motherboard to the prior stage to the connector.

The construction of the transmission lines contains two types of lines. The first is the breakout (BO), where these are the lines that come from the motherboard, that are nearby than the main route (MR) lines. They are used to connect the motherboard with the PCIe connector. The target impedance of the lines must be 85 Ω in differential mode. For calculate this impedance, a microstrip calculator was used with a guide of the variables in figure 3.2. The next dimensions to build the lines were used and are shown in the table 3.2, where the length variables are in mil [35]:

Table 3.2: Specifications of the transmission lines

Tline	**Trace Width (w)**	**Trace Separation (d)**	**Trace Thickness (t)**	**Dielectric Thickness (h)**	**Dielectric Constant**
BO	3.5	4	1.9	2.75	3.7
MR	4	4	1.9	2.75	3.7

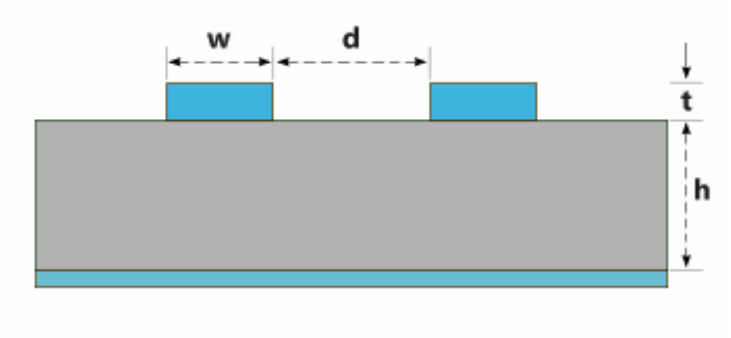


Figure 3.2: Guide of the variables of the table 3.2. Taken from [35]

The impedance through the line for the BO is approximately 84.96 Ω and for the MR line is 79.42 Ω. It is important to consider that the calculator assumes ideal widths of the line. It means that the EDW doesn't exist. The EDW is the settling of the copper. The impedance of the line by the effect of this settling is influenced. The EDW for both models is 0.5 mils on each side of the line.

Four differential pairs for both models have been modeled. A length of 500 mils for the BO model and 1000 mils for the MR model. In figure 3.3 is observed the differential transmission line built in HFSS, where this model was excited by *Waveports*. This port can be seen as the transparent sheet. The criterion in terms of height and width for the port is

15 times the thickness of the dielectric and the reference plane for the height. While for the width is 10 times the width of the trace, if the width of trace is higher than the thickness of the dielectric [44]. The port is started from the reference plane and goes up to the signal layer. The port is depicted in figure 3.4.

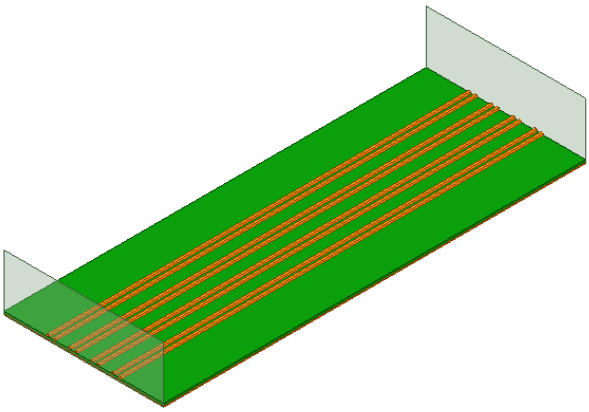


Figure 3.3: Differential Transmission line for the BO model from HFSS

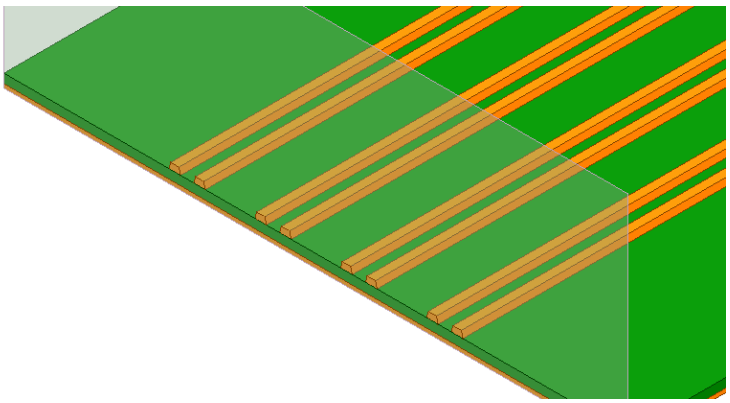


Figure 3.4: Port assignment of the differential line

The results to analyze of each line are the return loss, insertion loss, crosstalk (NEXT and FEXT) and the response in the time domain (TDR). In figure 3.5 are shown the measures mentioned. At first look, the line has the typical behavior of a transmission line. The reflection parameter has periodic resonances, while the transmission parameter decreases as the frequency increases.

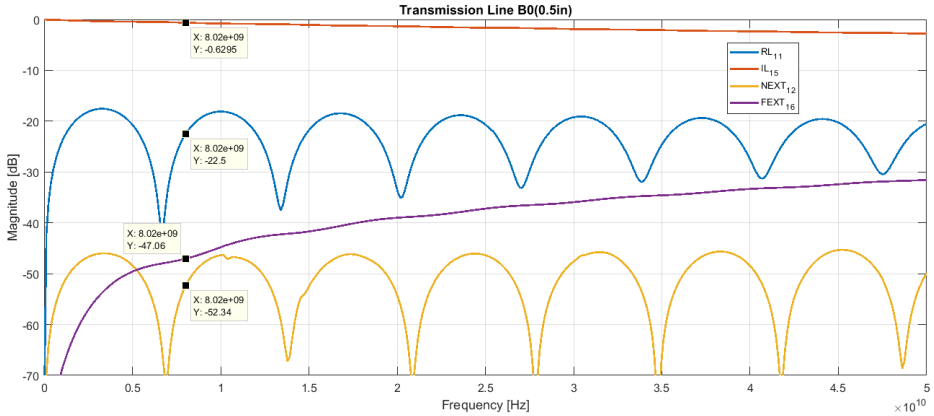


Figure 3.5: S Parameters of the breakout transmission line

From figure 3.5, most of the power is transmitted. Besides the reflection is below the -15 dB, so is complying with the criteria for the BO stage. Also, the crosstalk doesn't affect a lot this line, because is below the reflection parameter. To verify the impedance of the line, a TDR analysis is used to check the response of the line due to a stimulus. This can be shown in figure 3.6, where the impedance is below the 88 Ω, which is near to the target impedance of the system.

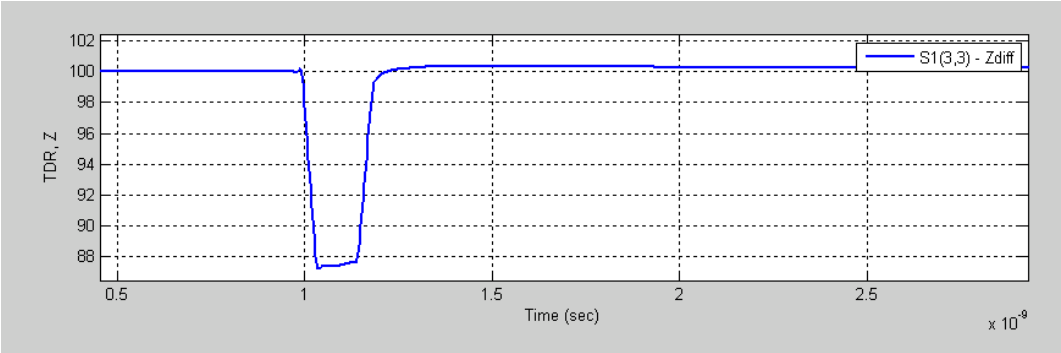


Figure 3.6: TDR response of the breakout transmission line

All the models that were built contemplate a loss model. As the materials that are used are dependent on the frequency. So to get a better approximation and result, these loss model are used. Exist different loss models as [45]-[46]:

- Debye: It is referred to the relaxation response of a dielectric medium to an external, oscillating electric field. This relaxation is often described in terms of permittivity as a function of frequency, which can be described by the Debye equation. This equation is usually expressed in the complex permittivity ϵ of a medium as a function of the field's frequency ω. HFSS allows specifying an upper and lower measurement frequency, and the loss tangent and relative permittivity values at the same frequencies.

- Piecewise Linear: This defines the material property values as a restricted form of a piecewise linear model with exactly 3 segments (flat, linear, flat). It must be specified property's values at an upper and lower corner frequency. Then between these corners, the software linearly interpolates the material properties. Above and below the corner frequencies, the software (HFSS) extrapolates the property values as constants.
- Multipole Debye: The software dynamically generates frequency dependent expressions for relative permittivity and loss tangent from the data of the relative permittivity and loss tangent versus frequency.
- Djordjevic-Sarkar: This model loss is used for low loss dielectric materials commonly used in PCB's and packages. This model uses an infinite distribution of poles to model the frequency response.

The loss model Djordjevic-Sarkar is used, because for this model only needed a specific value of the dielectric constant and the loss tangent at a specific frequency. The Debye model needs two values of the same characteristics at different frequencies, which implies inaccuracy in the models. The values of the table 3.1 were measured at a frequency of 5 GHz.

To get more accurate with the models, a roughness model was set. The roughness is a representation of the traces through small spheres, to set the roughness in HFSS the radius of the spheres and the Hall-Huray Surface Ratio must be known, which are a relation between the trapezoid area, the number of the spheres that will be modeled and the radius of the same. These data were provided as all the previous data and the radius that were used in the models was 0.5 μm and a ratio of 1.78.

The next transmission line is the main route line and was modeled. This with a length of 1000 mils. The line is depicted in figure 3.7, and the biggest difference of this model respect BO is that this uses different widths mentioned in table 3.2, as well as the length of the line. The dark green layer of the model is the soldermask, which is above the traces. In this model is shown in comparison with the BO model, due it was necessary to first show the transmission lines. And for this one, to verify that all models use all the layers mentioned in table 3.1. The S parameters are shown in figure 3.8. For the excitation, waveport was used and has the same criteria as the BO model.

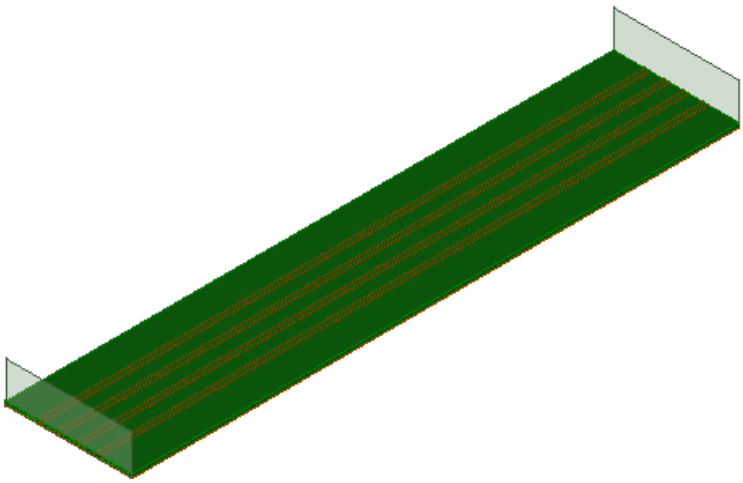


Figure 3.7: Main Route transmission line model

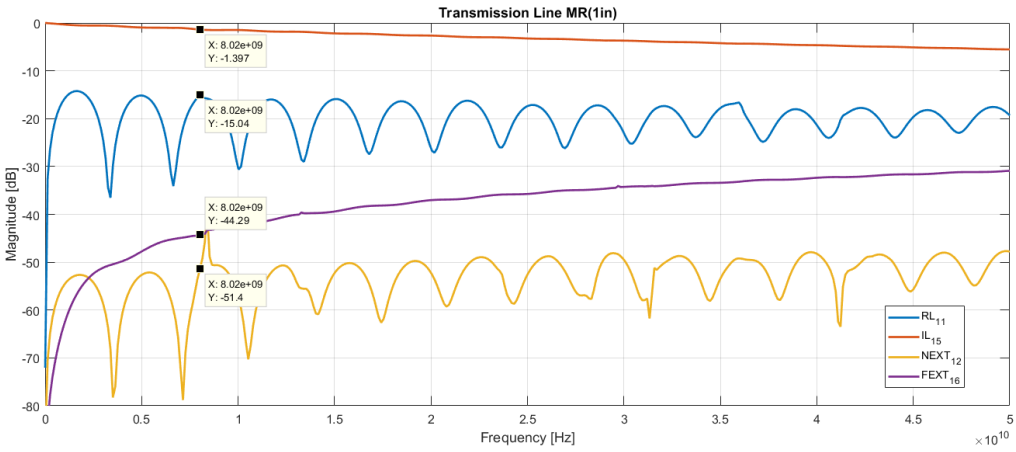


Figure 3.8: S Parameters of the MR model

As it is observed in figure 3.8, the transmission is -1.397 dB that represents most of the transmission of the power at the fundamental frequency of 8 GHz. Besides, the crosstalk doesn't affect the adjacent lines because the coupling between the differential lines is low. The response in the time domain of this line is shown in figure 3.9. The line has a resistive behavior due the graph is below of the target impedance of 85 Ω, approximately the line is in 83 Ω and doesn't have great changes during the stimulus. The graph was taken from HFSS.

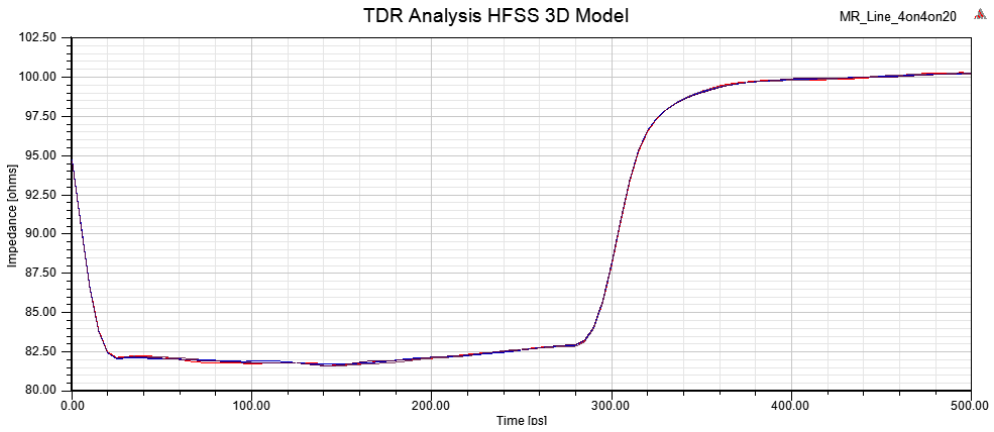


Figure 3.9: TDR analysis for the MR line

Ansys HFSS can model geometries from their 2D views. It is an option to get faster results, assuming that the 2D section does not change over time. An advantage of this solver is the time that it takes to simulate a model, it is around 30 min or less. While a 3D project could take at least a couple of hours. Besides, the computational resources that are used, are also bigger. This option to model 2D views is only for transmission lines because all the layers have the same length (depth). The 2D solver of HFSS can describe the line from their RLGC parameters that in the end can be transformed to S parameters.

Also, the breakout (BO) and main route (MR) lines with the 2D tool were modeled. First, the results of the BO will be shown, in figure 3.10 is observed the model. The excitations have to be assigned to the conductors. In this case, exist eight conductors and the reference plane, which is in the bottom layer. The results either the RLGC matrix or the S parameters can be extracted, where it just necessary define the depth of the line and the reference impedance. The results of the 2D BO line are shown in figure 3.11.

Figure 3.10: 2D view of a section of the BO model

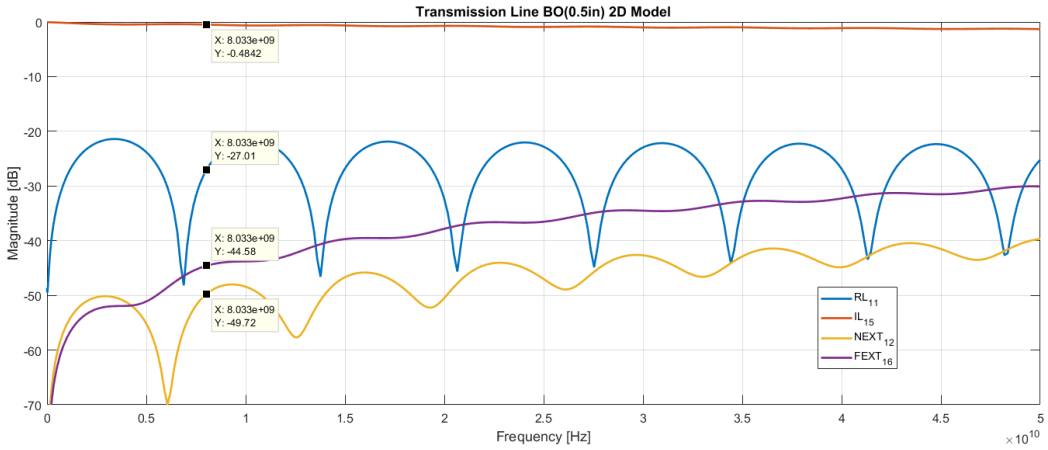


Figure 3.11: S Parameters of the 2D BO model

The results of the figure 3.11 shown the same trend as the results of the figure 3.5. It implies the most of the power is transmitted. The same happens with the crosstalk, it is observed that the next and fext don't influence on the rest of the lines. To approximate this line the Djordjevic-Sarkar loss model was used, with the reference measurements that have been provided. The 2D models can't be applied an analysis in time domain, the TDR analysis can use only in 3D models. In figure 3.12 is shown the 2D MR model, where this model is very similar to the 2D BO model. The difference is in the length and the width that the lines have. It is specified in table 3.2 and figure 3.13 is shown the results of the main route model in 2D.

Figure 3.12: Section of the 2D MR model with a length in the outsider lines of 50 mil in each side

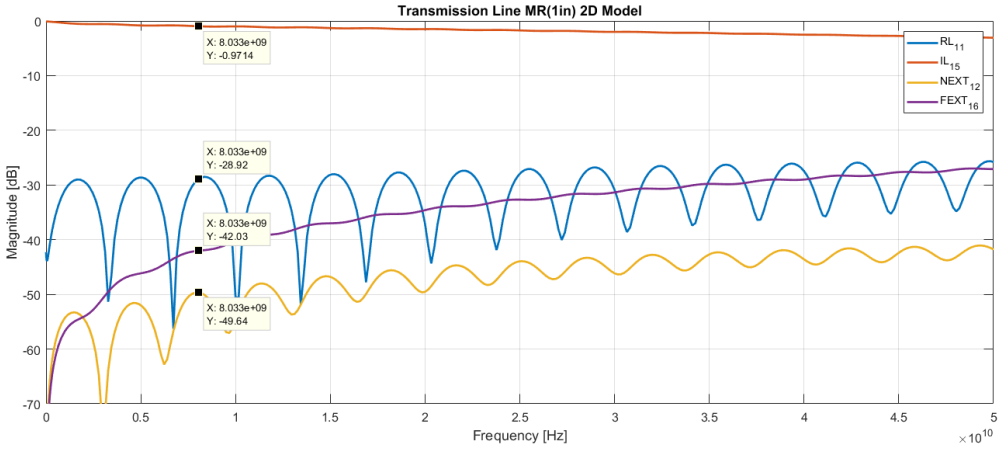


Figure 3.13: S Parameters of the 2D MR model

This result using the Debye loss model was obtained. Due the Djordjevic-Sarkar model also was used and the power was -40 dB, which it is something desirable but far away from the reality. Even these results are far from the results obtained in figure 3.8. The lines have a high transmission and a low reflection. To set the Debye loss model in the prepreg layer the next data were used:

- Frequency: 1 GHz as lower and 8 GHz as higher
- Dielectric Constant: 3.5 as lower and 3.7 as higher
- Loss tangent: 0.015 as lower and 0.017 as higher

For the soldermask layer the Debye loss model was approximated with the next data:

- Frequency: 1 GHz as lower and 8 GHz as higher
- Dielectric Constant: 3.2 as lower and 3.4 as higher
- Loss tangent: 0.029 as lower and 0.031 as higher

Something to consider is that the Debye loss is an approximation. The measures at different frequencies is unknown. For this case, the other value was put with some criteria. To get accuracy, measurements at different frequencies must be made to use in the right way this loss model.

3.4. Via Model

This subsection contains the built of a via. In chapter 2 was mentioned that can be ground via or signal via. For the modeling, the dimensions of the diameters of the different cylinders that compose the vias and spacing between them are shown next. The data were provided and are shown in table 3.3:

Table 3.3: Specifications for the construction of the vias

Section	Dimension (mil)
Drill	12
Pad	22
Antipad	32
Thickness pad	Main trace's thickness
Thickness drill	2*(prepreg's thickness + reference's thickness) + core's thickness
Pitch between Negative and Positive via	30
Distance between differential vias	60
Distance between differential vias and ground vias	30

All these elements, have different proposes that were mentioned in chapter 2. For example the antipad, drill, pad and ground vias. Figure 3.14 is shown the via model. The only element that isn't mentioned in the figure is the antipad. This was described previously and is a dimension that only applies to the signal vias and not for the ground vias. The spacings have to be respected because permit that the differential pairs don't influence in other pairs.

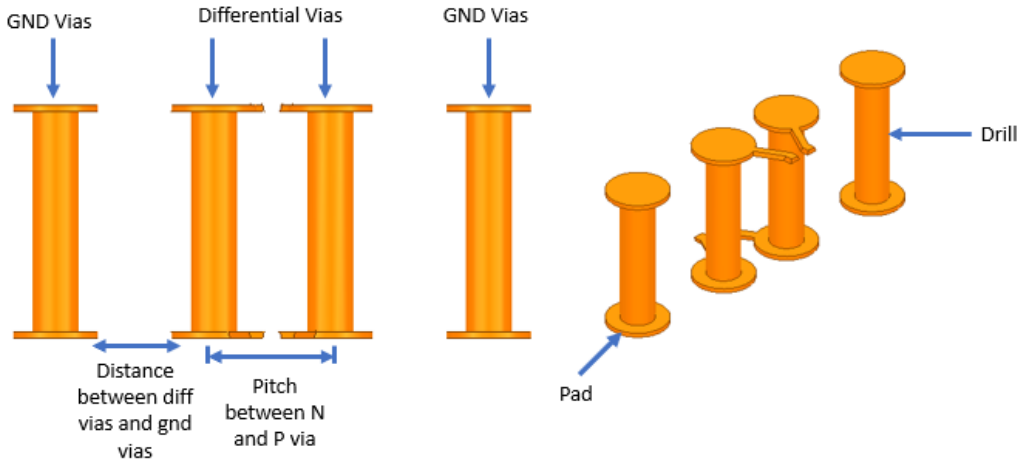
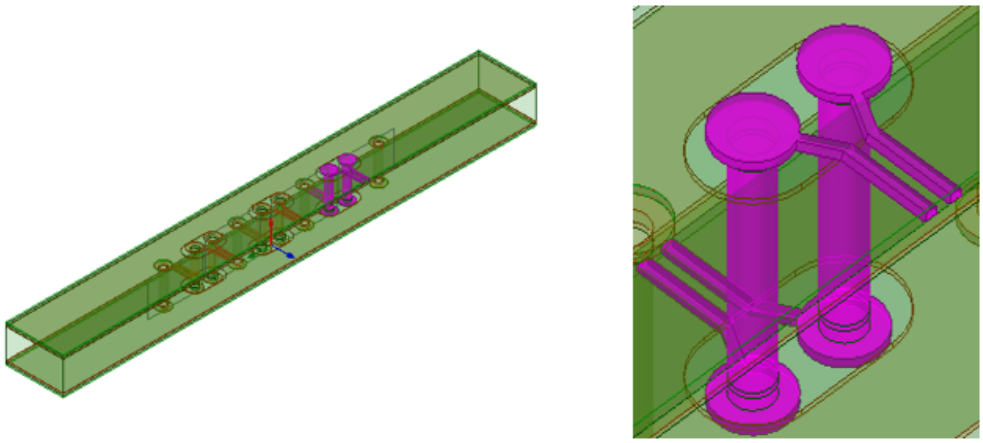


Figure 3.14: Via model built in HFSS

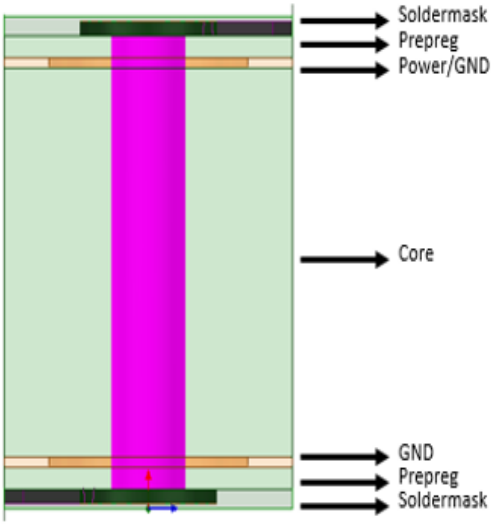
The vias were modeled as an array of three differential pairs, where between them are ground vias just like the figure 3.14. This model has all the layers, because the vias are through hole in the PCIe buses models. Due only the vias are modeled, and for the excitations are using waveports and are on the edges of the radiation box, imply that the traces which are out of the via, can't have a considerable length. This would introduce transmission

lines effects because also would modeled the access lines. Also as part of the simulations results, a model with a card with more width is attached, the same as the length of the card.

Figure 3.15 are shown two subfigures, in the subfigure *a* is shown the model realized in HFSS, with the ground vias and the differential vias. The length of the trace outside of the antipad is 27.5 mil. Also can be shown the extraction of the antipad in the copper layers, which are the inner layers of the stackup. In the subfigure *b* is shown a front view of the board of the via and can be observed all the layers of the stackup and how these are distributed.



(a) Whole design and extraction of the antipad in the copper layers



(b) Stackup of the vias with a frontal view

Figure 3.15: Via model built in HFSS

The simulation results will be shown below. The same electrical parameters and a TDR analysis will be analyzed to see the behavior and impedance of the via. Figures 3.16 and

3.17 are showed the analysis in frequency and time respectively.

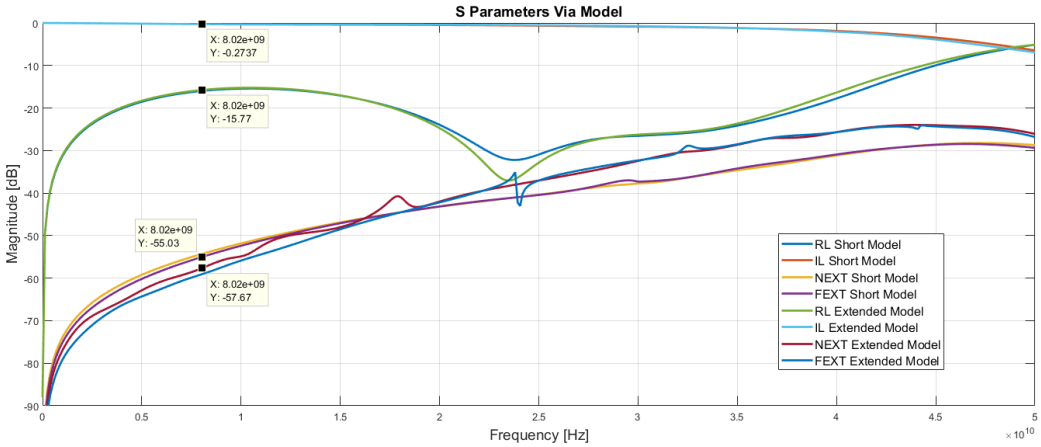


Figure 3.16: S Parameter of the via modeled in HFSS

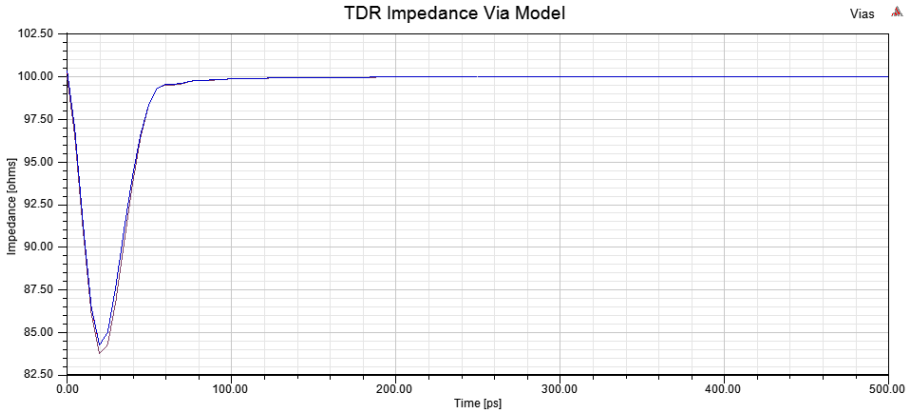


Figure 3.17: TDR test apply to the via model built in HFSS

A bandwidth up to 40 GHz with a loss of -2 dB for the response in the frequency domain of the via is shown. Most of the power is transmitted and the minimum of the power is reflected. While the crosstalk doesn't have a considerable influence in the pairs of the board. Hence, for the fundamental frequency of the PCIe 4.0, the via operates with the minimum lost power. The response in the TDR is observed in figure 3.17. The small behavior of the transmission line that the model has is observed. After that the response, in an inductive is changed because the graph starts to go up as a normal inductive element saw in chapter 2.

3.5. DC-Blocking Capacitors

This subsection consists of the characterization of the DC-Blocking capacitor. The principal function of the capacitor is blocking the DC component and decoupling the signals

between the transmission and reception stages. The goal is to model the losses that a capacitor can generate in high frequency, due at high frequency the behavior of the capacitor is totally different at DC. This subsection will show the 3D model in HFSS as the results obtained from the simulation.

To get results near at the segmented models, a capacitor model was provided. It is with the standard of 0201, and is different to the mentioned in chapter 2 but has a capacitance permitted in the standard that the PCIe buses use. This capacitance is 220 nF. As mentioned, it is looked to model the high frequency loss, for that a library was used. It's just necessary to put the standard of the capacitor and the normal value of the same and the library provides the values of the lumped elements of the capacitor.

From the library, the inductance has a value of 177.865 pH and the resistance has a value of 27.918 mΩ. In figure 3.18 is shown the 3D model of the capacitor, where the principal parts of the same are marked. These are the metal contact, the RL lumped components, the pads and the lumped ports. The model with lumped port is used because the model was defined to approximate without transmission lines. Also, an advantage of this is that it's not necessary to put the port in the edges of the radiation box. It is had a certain flexibility to model the component with more area for the other layers. The model that was simulated is depicted in figure 3.19 with the prepreg, soldermask and reference layer.

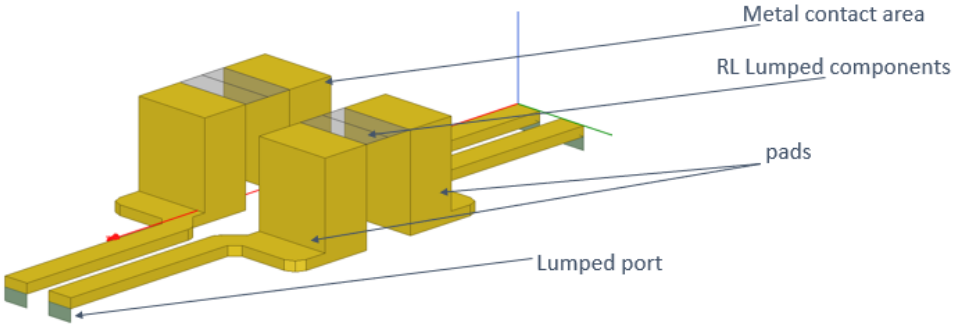


Figure 3.18: 3D model of the DC-blocking capacitor

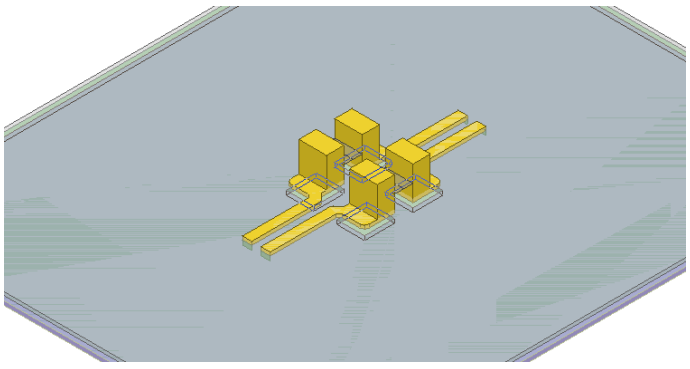


Figure 3.19: 3D model of the DC-blocking capacitor simulated in HFSS

As appreciated from figure 3.19, the reference layer has four extractions, which exactly have the same measures of the capacitor's pads. This is realized to ensure the minimum reflection of the power by another factor that doesn't be itself. The modeling of the lumped elements was realized with an assignation of *lumped RLC element* that HFSS has. When chosen this assignation, just the value of the lumped element is defined and reviewed that the current flow goes on the same way for both lumped elements (R and L). The position of the lumped elements could be three and are the top, middle or bottom of the capacitor. The middle was chosen to have the middle result of the capacitor and not have an extreme result due to the position of the lumped elements. The lumped element (R) assignation is shown in figure 3.20, wherein the other rectangle that is below is the assignation of the inductance element.

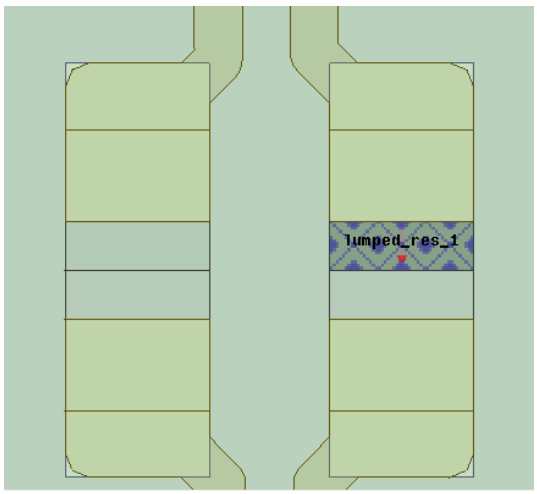


Figure 3.20: Assignation of lumped elements, top view

The results of the model are shown in figure 3.21. In general, most of the power is transmitted at the fundamental frequency. The losses that are generated by the capacitor, doesn't affect a lot in the transmission. It will be necessary to corroborate this measure with some complex cases, where involves transmission lines and capacitors as a first approach. A problem with this model is that can't be generated a TDR analysis because the ports utilized were lumped type. This implies that the port can't read the nearby lines that could be transformed in differential pairs. Besides, only one differential pair is modeled and by that, the crosstalk in differential mode can't be analyzed. So only was analyzed in single mode and was shown in figure 3.21, where the influence of the crosstalk is despised it.

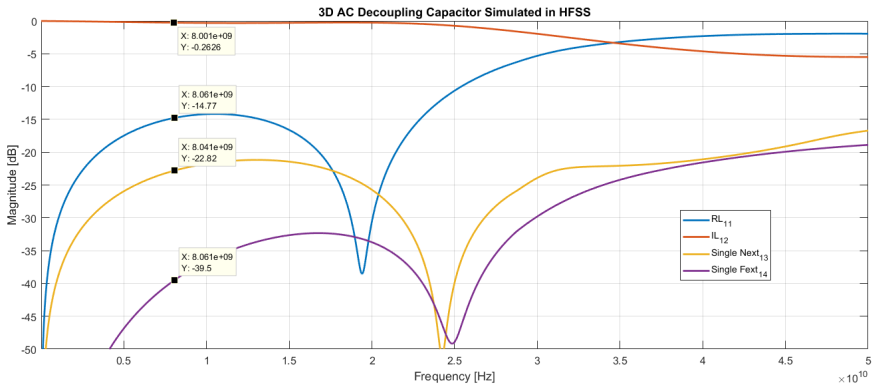


Figure 3.21: S parameters of the capacitor with two lumped elements modeled in HFSS

Another model was executed to include a third lumped element that was the capacitance with a value of 135.932 nF obtained from the same library. The results are shown in figure 3.22, and in comparison with the previous results, the big difference is the reflection. These are increased and are expectable because the model has more losses than had before. But for the fundamental of 8 GHz, the reflected energy is minimum. Also, in this case, a TDR cannot be applied due for the same reasons as the two lumped element model.

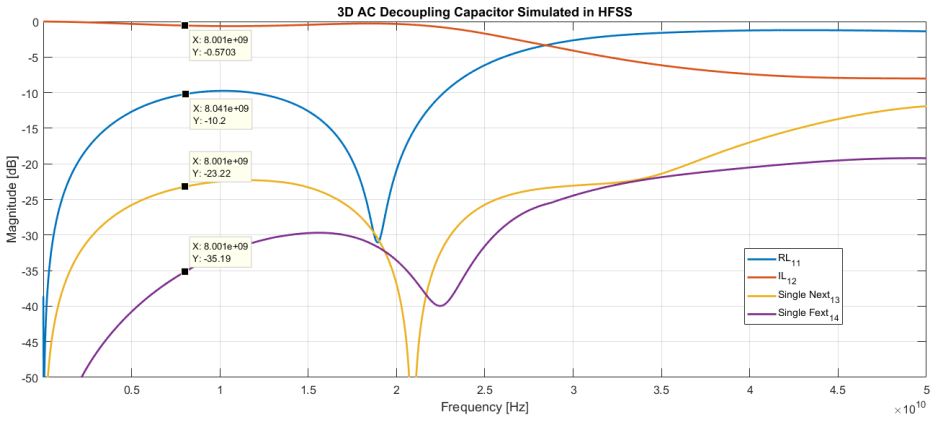


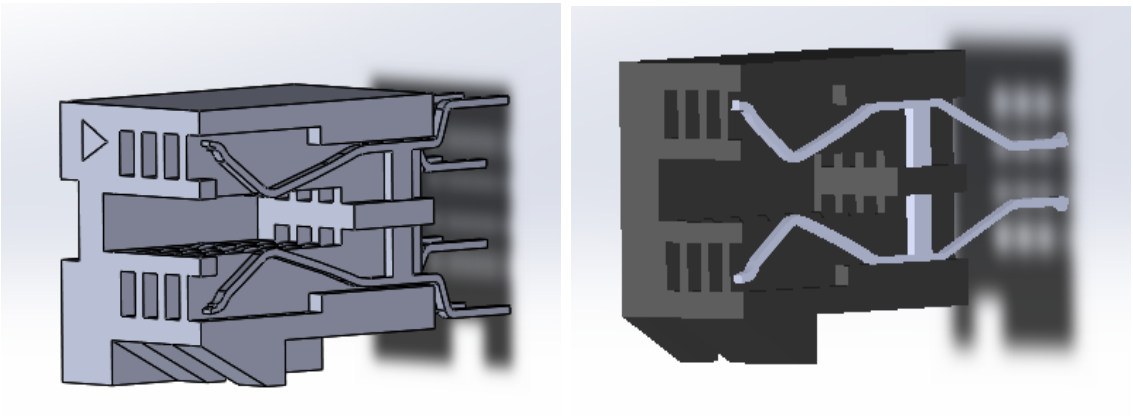
Figure 3.22: S parameters of the capacitor with three lumped elements modeled in HFSS

3.6. PCIe Connector

This subsection contains a first reach of the PCIe connector 4.0. The models that were used to simulate the PCIe connector will be shown. Between the models that were used, are the through hole connector and the surface mount connector.

To model the PCIe connector, from Solidworks was modeled to take a section of the connector. Solidworks is a CAD software for mechanical modeling in 2D and 3D. The software is able to model pieces and sets and get sections of the whole piece as the PCIe connector [47]. In figure 3.23 are shown two types of connectors that were used in the simulations.

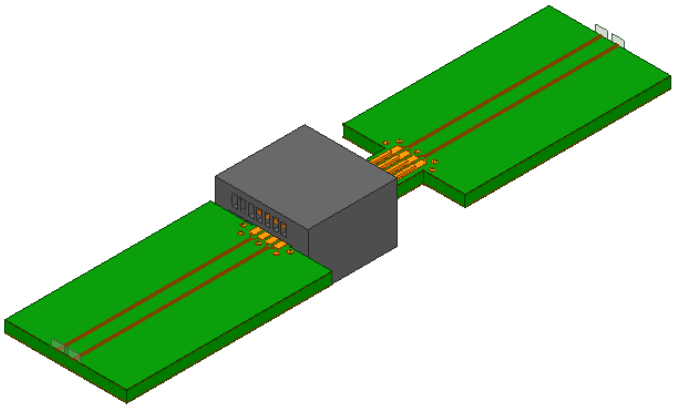
The connectors are a section of a PCIe connector with 36 pins, and two differential pairs will be modeled.



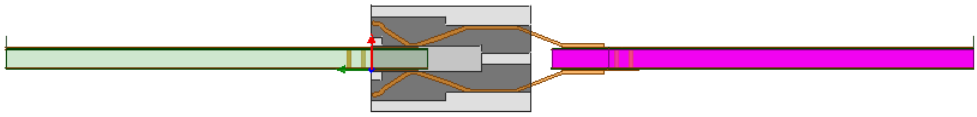
(a) PCIe Connector Through Hole (TH) model (b) PCIe Connector SMT model

Figure 3.23: PCIe connector obtained from Solidworks

For the simulation of the SMT model, a card is embedded in the connector. This card has pads with a dimension of 0.7 mm with a difference between pads of 0.3 mm. This is the measure that the footprints of the connector provided. In figure 3.24 is observed the channel with the PCIe SMT connector model in HFSS. The injection of the signal is through waveports. As it is observed in the figure 3.24, the ground vias are as near as possible of the connector stage, this to avoid losses in the transmission stage. The same pattern is observed in the reception stage.



(a) Channel with a PCIe SMT connector

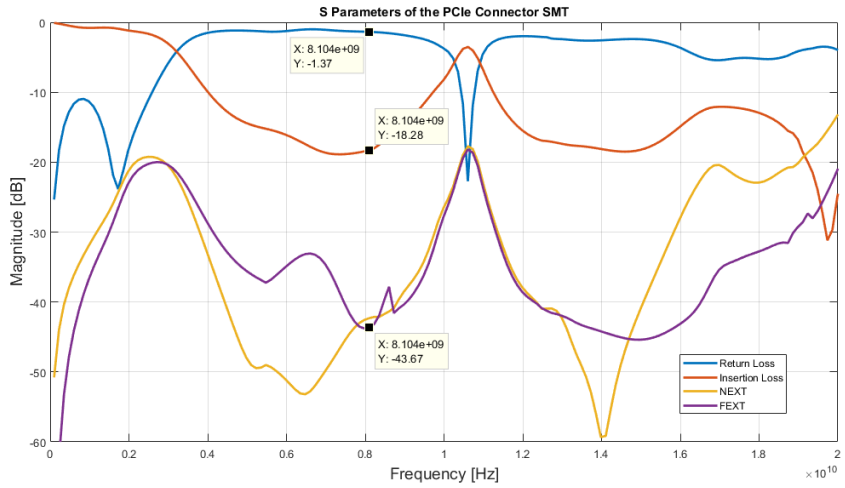


(b) Side view of the channel with the PCIe SMT connector

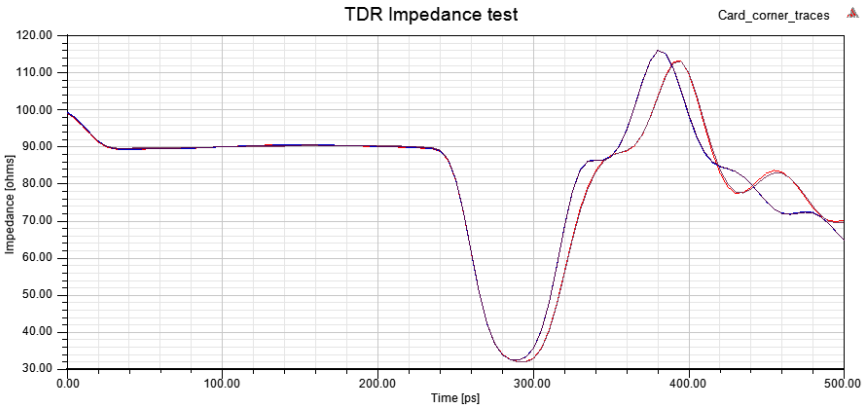
Figure 3.24: PCIe SMT connector simulated in HFSS

The results of the simulation of the channel of figure 3.24 are depicted in figure 3.25. It can be observed that the transmission has minimal power loss until 3 GHz approximately. After, the reflection is higher and practically most of the energy is reflected. The model with this connector doesn't comply with the PCIe transmission specifications for a fundamental frequency of 8 GHz. The configuration of the pins assignment is with the signal pins in the upper side of the card, and in the lower pins are of reference.

With the TDR analysis can be observed that exists a mismatch between the stages of the connector and the transmission and reception cards. This is presented because the impedance has an abrupt change from 90 Ω to 30 Ω. It represents a big problem because can't exist huge changes in the impedance, and the rest of the graph of the TDR conserve those abrupt changes. Possible reasons for the low transmission that the channel has could be the pins distribution between signal and reference. Also, the lines that are used to transmit the signal implies a great difference with the lines of the embedded card due to the width of them. A mismatch between the lines is created that in the end is an impedance decoupling.



(a) Channel with a PCIe SMT connector



(b) S Parameters of the channel with PCIe SMT model

Figure 3.25: Simulation results of the channel with PCIe SMT connector

The next simulation is about the through hole connector. It is the connector that is used in the PCIe buses of a personal computer. First, only the PCIe connector with the port assignment in their pins and through transmission lines was simulated with an embedded card. A correction in this simulation was made with respect to the previous channel and this is the distribution of the pins. This time the order given for a 36 pins connector has followed. In table 3.4 the distribution of the pins of the PCIe is mentioned. There exists a great difference in comparison of the distribution for the SMT connector realized as first approach. In both rows of the connector, exist ground pins and not just in one row. In figure 3.26 is depicted the distribution of pins of a PCIe connector, where the upper row is *A* and lower is *B*. In the same way, only two differential pairs are modeled.

Table 3.4: Pins distribution of a PCIe connector

Row	Pin 13	Pin 14	Pin 15	Pin 16	Pin 17	Pin 18
A	.	-	GND	Signal (+) Rx Data	Signal (-) Rx Data	GND
B	GND	Signal (+) Tx Data	Signal (-) Tx Data	GND	-	-

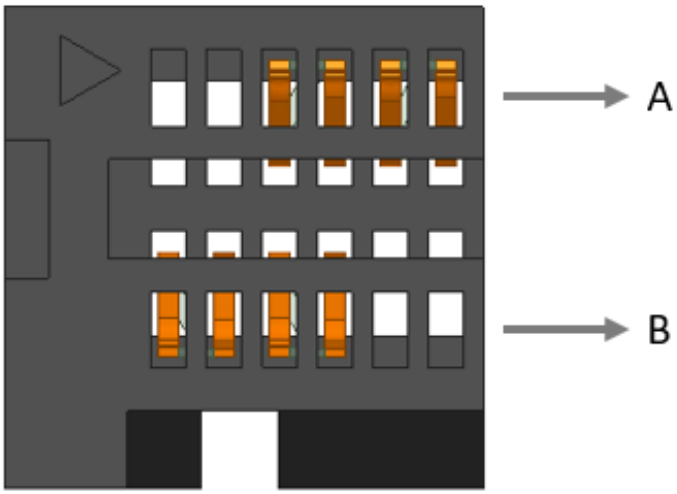


Figure 3.26: Rows assignment of a PCIe connector

The first simulation with the through hole connector is only the connector and their pins as is observed in figure 3.26. The injection of the signal is through lumped ports. The assignment between a reference pin (outside pins of the row) and a signal pin (inside pins of the row) is realized. The results of the connector are shown in figure 3.27. The same problem exists as in the SMT connector and this is the power transmission that the bandwidth is not the expected. Since at a frequency of 2 GHz the reflection becomes higher. As it is observed the crosstalk is higher in comparison with previous models that were mentioned but still be minimum the influence of the lines between them. Also, the peaks in the crosstalk graph are for the lack of passes of the simulation. The simulation was realized with lumped ports and it can't be obtained the TDR analysis, but a reference as in figure 3.25 can give an idea about what is happened in the connector, and this is a mismatch in impedance terms.

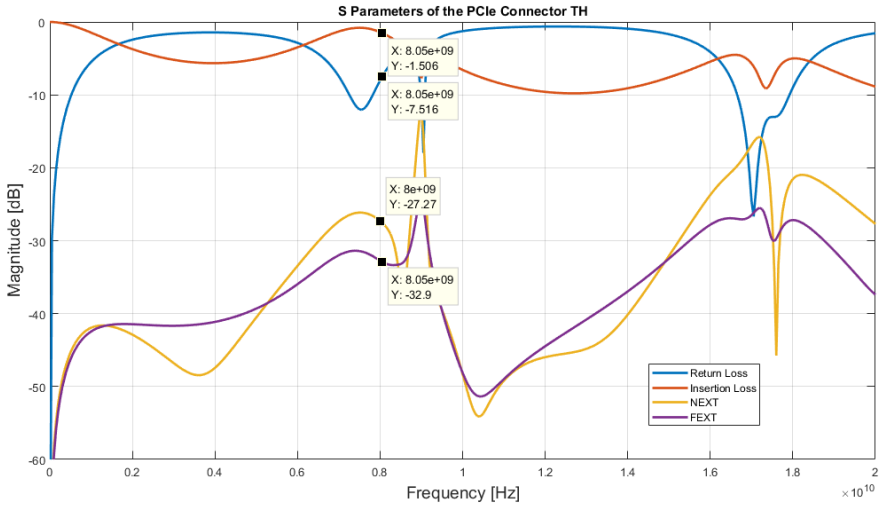
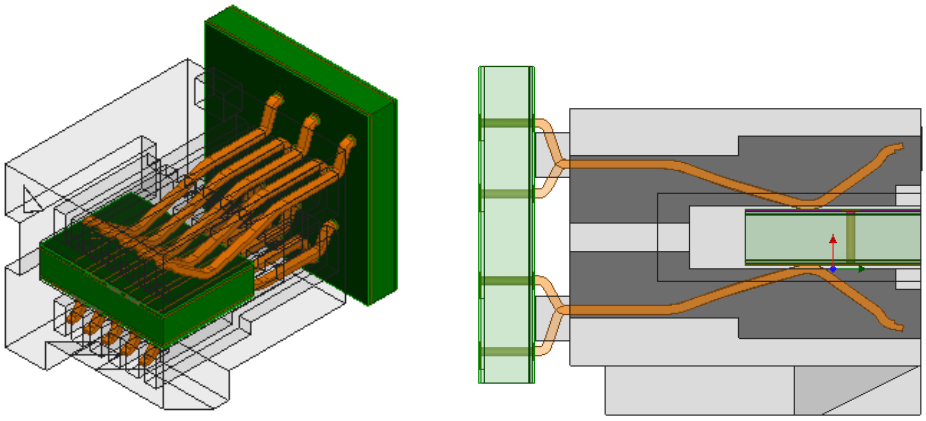


Figure 3.27: S Parameters of the simulation of PCIe connector without embedded card

For a second simulation with this type of connector, a little card in the connector was introduced. Also was put a little card in the reception stage, and signal vias and reference vias were used for the second card. This description is observed in figure 3.28. The results are observed in figure 3.29 and are very similar as figure 3.27. The union of the reference pins didn't help a lot because a little more of reflection in a higher bandwidth instead to reduce it was created. In general, the bandwidth for the PCIe connector is not the expected. This could be because is only modeling a section of the PCIe connector and could be necessary to model the whole connector.

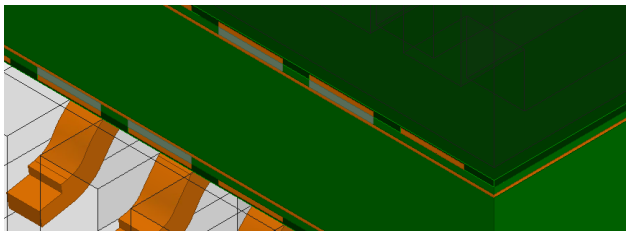
As discussed, some tests have been realized, where all the simulations have not the expected bandwidth. A channel with considerable lengths was modeled and failed in the transmission at 3 GHz. The other simulation consisted of the connector without cards, and the result was the same, even a little worst because the cut off frequency was in 2 GHz approximately. The final test didn't help a lot because even with all the reference pins landed in the same reference plane, the transmission didn't increase in terms of bandwidth.

A problem with this simulation is the environment in how this connector was simulated. It is unknown because the info only references the dimensions of the connector and the footprint. Something difficult to assign in this interface are the ports. As was observed in the connector without cards, this one didn't respond well, and the distribution of the pins was followed. With a bad assignment of the ports, implies that the results won't be the desirables.



(a) Isometric view of the TH connector with the card

(b) Side view of the channel with TH connector



(c) Injection of the signal through lumped ports

Figure 3.28: Model of the through hole connector in HFSS

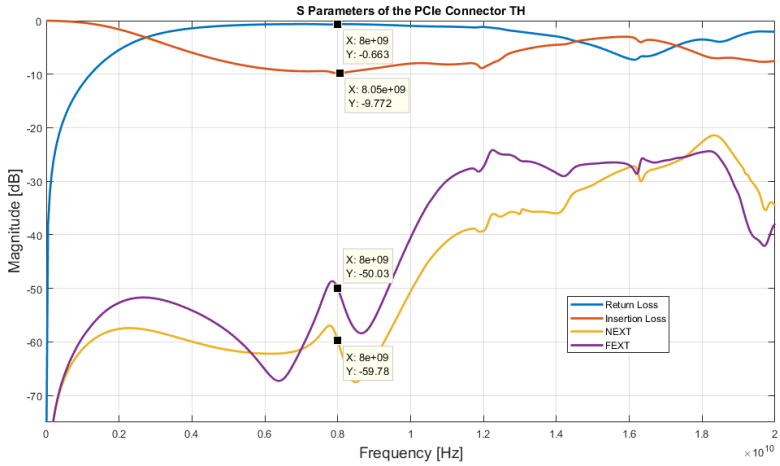


Figure 3.29: S Parameters of the simulation of PCIe connector with embedded cards

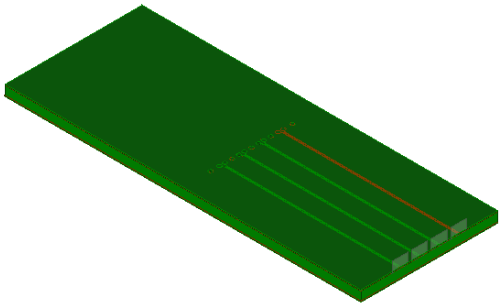
3.7. Combined Models

This subsection deals with the concatenation of the basics models that have been described as the transmission lines, DC-blocking caps and the vias. These models are the

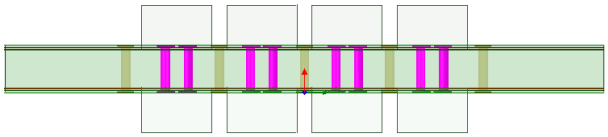
transmission lines and DC-blocking caps, transmission lines and vias. Finally, a channel with all the basic elements will be developed. As the previous simulations, these models conserve the features that were mentioned previously for the simulations as the broadband which covers, the sweep and the permitted error.

3.7.1. Transmission lines and Vias

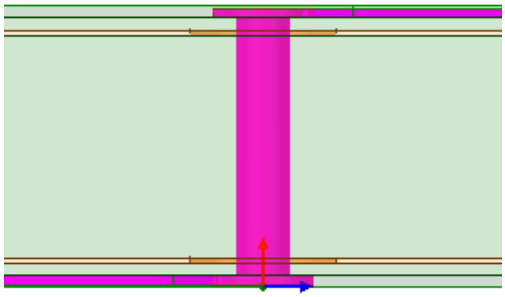
The first bigger model is the concatenation of transmission lines and vias. Four differential pairs will be modeled, with a length of 1000 mils on both sides of the card and in the middle are the vias that are through hole type. The transmission line with the main route specifications is modeled. It has a width of the trace of 4 mils and the remaining of dimensions are conserved from the breakout model. The injection of the signal is given through waveports. In figure 3.30 are depicted different views of the model, as well as the waveports. Also the ground vias can be observed, which are between the differential pairs.



(a) Isometric view of the TL, Via and TL model



(b) Side view of the TL, Via and TL model

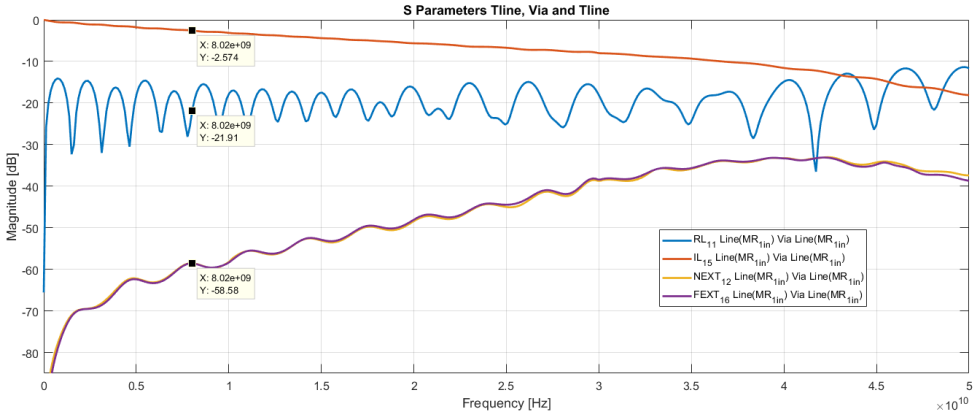


(c) Front view of the TL, Via and TL model

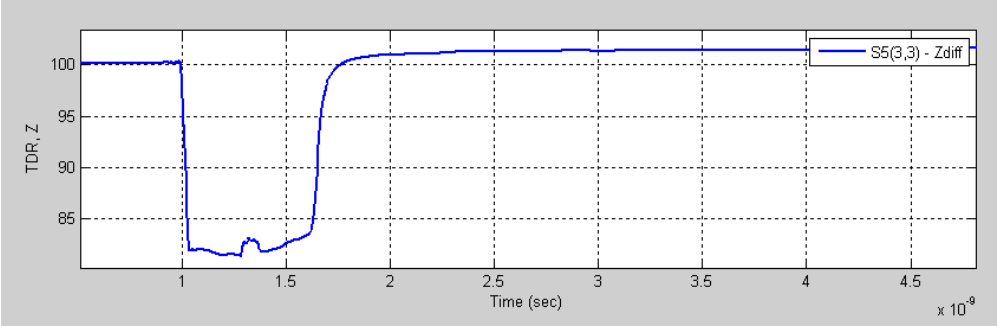
Figure 3.30: Transmission Line, Via and Transmission Line Model simulated in HFSS

The results of this model are shown in figure 3.31. The description of the model through the S parameters and the check of the impedance in the time domain is included. From

the results in the frequency domain, the effect of the vias is noticed. Due the losses in high frequency are bigger. A little mismatch are generated by this vias. A reduction of -2 dB approximately in the transmission of the power is produced. The reflection has the same trend respect the rest of the graphics that have been shown. The crosstalk as it is observed don't have a considerable influence in the rest of differential pairs.



(a) S Parameters of the TL, Via and TL model



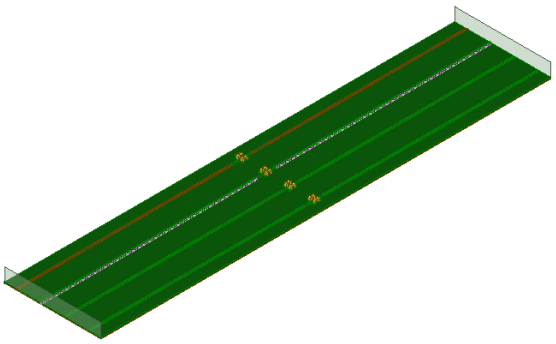
(b) TDR test of the TL, Via and TL model

Figure 3.31: Behavior of the model described by their S parameters and TDR test

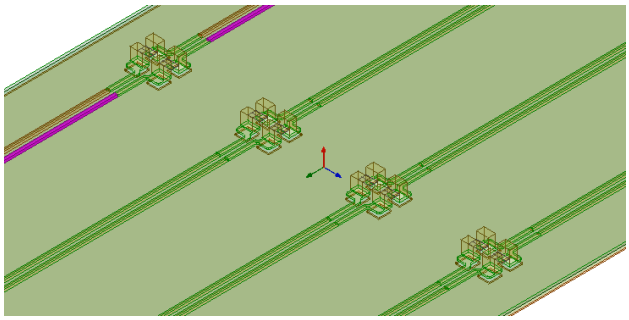
The TDR analysis in figure 3.31 is observed, the reason for the increase in the losses in high frequency, is because the vias contribute an inductive effect and in the rise of the graph can be appreciated. After the signal passes the via and continues through the transmission line, the stability is observed because a lot of peaks or abrupt changes isn't presented. In terms of impedance, the model is approaching to the target impedance. With the S parameters are shown that impedance isn't critical given the transmission at least at the fundamental frequency is stayed.

3.7.2. Transmission lines and DC-Blocking Capacitor

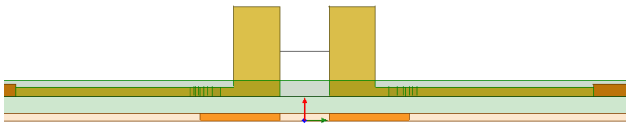
The next model that will be concatenated are the transmission lines with the DC-blocking capacitors. As the transmission line and the via model, will be executed with transmission lines of the main route type in both sides and in the middle will be the DC-blocking capacitors. The length of the lines is 1000 mil each one. The extraction of the pads below of the capacitors in the reference layer must be realized. In figure 3.32 are observed different views of the model, wherein the first subfigure is the whole model. The second subfigure the extraction pads in the reference plane can be appreciated. In the third subfigure a side view is observed, where the lumped elements are shown. The excitations were realized by waveports.



(a) Isometric view of the TL, DC-block cap and TL model



(b) Visualization of the capacitors and the extraction of the pads in the reference layer

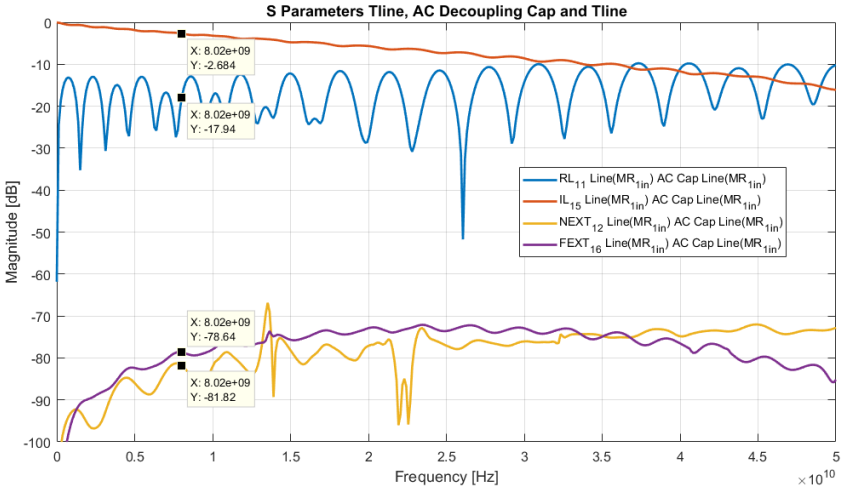


(c) Side view of the model and the lumped elements between contact areas

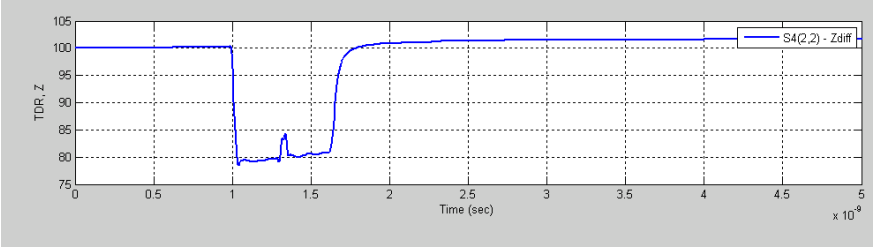
Figure 3.32: Different views of the model TL, DC-block Capacitor and TL; and the lumped elements between the metal contact areas

In figure 3.33 the results of the simulation are shown. The first subfigure is depicted the S parameters, while in the second subfigure the analysis in the time domain is shown. The results in the frequency domain are presented, with similar results in terms of losses as the model with the vias. This is expectable due a capacitor is modeled and this passive element contributes more losses than the usual. The transmission and reflection are maintained acceptable with a value at a frequency of 8 GHz of -2.684 dB for the transmission and for the reflection a value of -17.94 dB. Most of the power is transmitted. While the crosstalk doesn't have a considerable influence in the other differential pairs. The peaks that are presented are given because the simulator needs more passes and a finer sweep to interpolate the results. This means that in the peaks of the graph's the solution wasn't the best.

Another fact to analyze are the results in the time domain. In the second subfigure of the figure 3.33, the TDR analysis is shown. As it is observed the impedance has a little more of loss respect to the target impedance and previous results. As commented this happens by the capacitor, because generates more losses than usual. Also as the capacitor with their inductive and resistive elements is modeled, it implies a rise in the TDR graph.



(a) S parameters of TL, AC decoupling capacitor and TL model

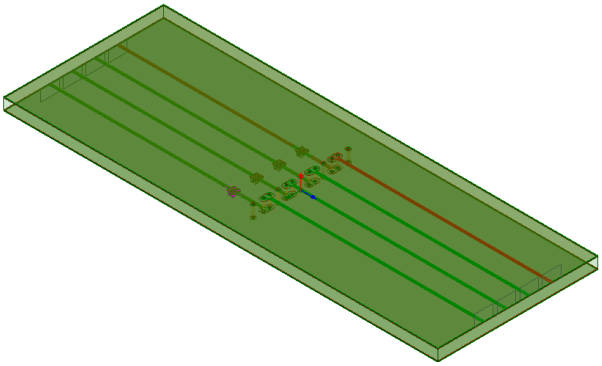


(b) TDR test of the L, AC decoupling capacitor and TL model

Figure 3.33: Frequency and time analysis of the TL and Capacitor model built in HFSS

3.7.3. Transmission line, Via and DC-blocking Capacitor

This section is related to the concatenation of all the basics models as vias, capacitors and transmission lines. For this model, with a transmission line of the main route type with a length of 1000 mils is started and with a via is finished. Then with another transmission line of the main route type is continued, the length of this line is 90 mils and with the DC-blocking capacitor is touched. The remaining stage is a transmission line with a length of 860 mils. The model was injected by waveports. Besides, as the other models that involve the capacitor, the assignment of the lumped elements must be realized, as the extraction of the pads in the reference layer. They are used the antipads to avoid a short on the model. All this description can be observed on figure 3.34.



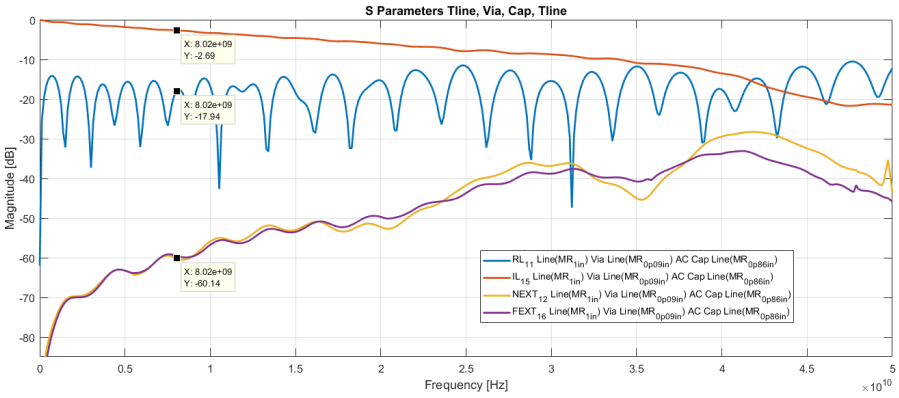
(a) Isometric view of the Tline, Via, Capacitor and Tline model

(b) Inclusion of the vias and the capacitor on the same model

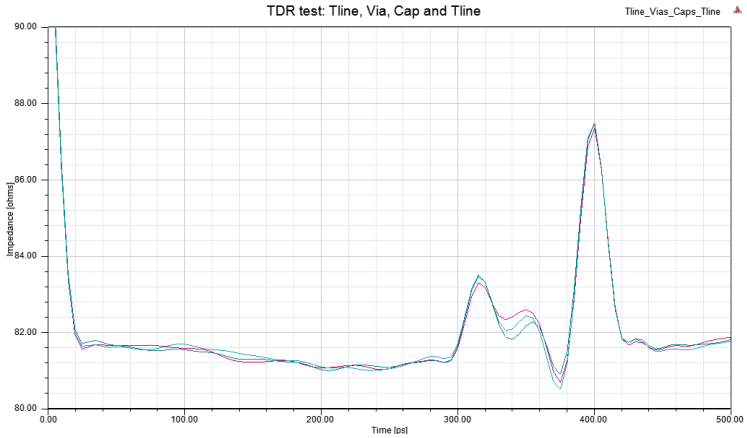
Figure 3.34: Model with involves transmission lines, vias and capacitors

The results of this model are shown below in figure 3.35. In terms of frequency, the biggest difference respect the model that involves two concatenated elements (transmission lines and vias), they are the losses that are presented in high frequency. Since 30 GHz, the transmission is below the -10 dB, while the reflection becomes higher above the -10 dB. Similar results as the concatenated models before the fundamental frequency are presented. The model doesn't present a lot of loss in low frequency, as in higher frequency does. The power at 8 GHz is -2.684 dB and the reflection is -17.84 dB. Once again the crosstalk is low, due are below the reflection, which means that don't affect in the different pairs that the

channel has.



(a) S Parameter of the model described in figure 3.34



(b) Analysis of the impedance with a TDR test

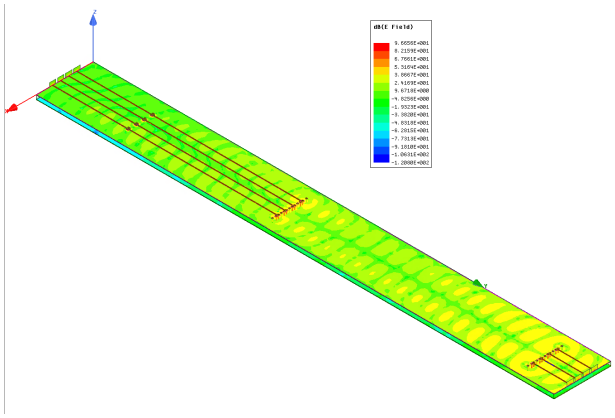
Figure 3.35: Simulations results that involve transmission lines, vias and capacitors

To analyze the impedance of the model the TDR analysis was applied. At the beginning the behavior is one of a transmission line (resistive). After that, the graph has a rise due to the vias, which have an inductive behavior with the transmission lines connected. The other rise is due to the capacitor because the inductive element is observed that the capacitor has, influences in a higher impedance. Nevertheless, the impedance in general terms fluctuates near of the target impedance.

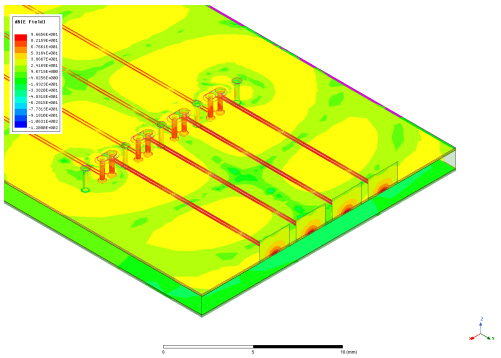
3.7.4. Full PCB Path

The final model that will be modeled is the concatenation of the transmission lines as main route and breakout, the vias and the DC-blocking capacitors. This model represents the whole channel from the motherboard and the entry before the PCIe connector. The diagram of this channel in figure 1.1 can be observed. The BO stage has a length of 500

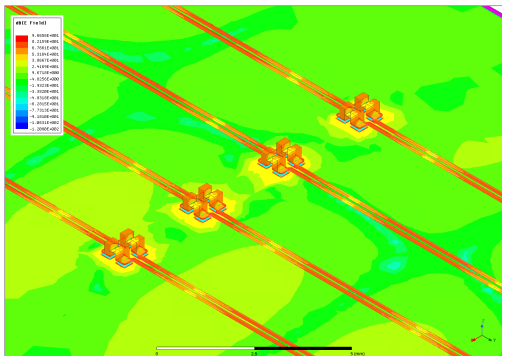
mils and with a stage of vias is connected. After that, a transmission line of the main route type is continued until a vias stage. This line has a length of 3500 mils. Its continued with the route and another transmission line of the main route type with a length of 2000 mils is connected with the capacitors stage. Finally, it is finished with a transmission line of the main route type of 1000 mil. In figure 3.36 can be observed by the magnitude of the electric field of the full channel model, where most of the energy flows through the line.



(a) Isometric View of the full PCB path model



(b) Beggining of the channel where the waveports can be observed, BO lines and the vias



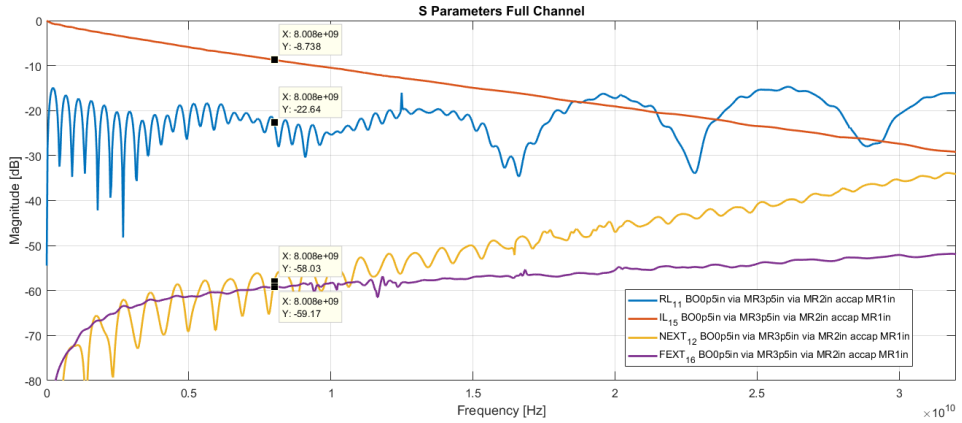
(c) DC-blocking capacitor stage in the full PCB path model

Figure 3.36: Full PCB path simulated in HFSS

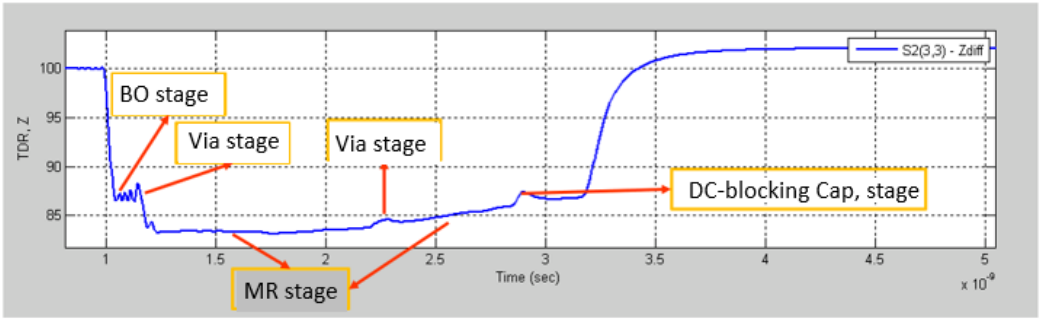
The results of this model can be observed in figure 3.37. For reduction of complexity, the solution to 32 GHz has been reduced. This happened because some problems with the computational resources were presented . Basically, in terms of memory because the mesh of the geometry is complex for all the elements as well fot the thickness, and length of the channel. The model was excited by waveports.

The frequency domain analysis is depicted in figure 3.37. This analysis shows the progressive losses in a very fast way due at that fundamental frequency, the value of transmission

is -8.73 dB. This value is approximately three times the value of the models, which concatenate two basic elements. The result is expectable due in the model is included elements, which generate more losses than the usual as the vias stages, the capacitor stage and mainly for the length of the channel which it is of seven inches. The reflection of the model at the fundamental frequency is -22.64 dB. It is shown that the problem is not in the match impedance, rather they are in the losses generated by the total length of the channel. Finally, the crosstalk doesn't affect the channel at low frequency but as the frequency increases the NEXT increases too. This means that differential pairs would have some negative effect between them.



(a) S parameters of the full PCB path model



(b) TDR analysis of the full PCB path model

Figure 3.37: Simulations results of the channel between the motherboard an the entry previous the PCIe connector

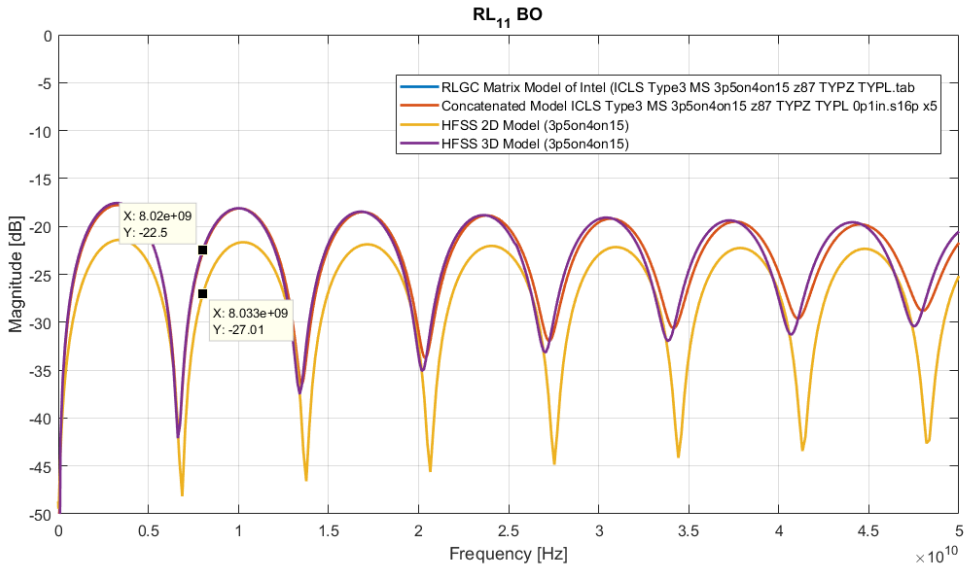
Finally, the TDR analysis can indicate how much a model is coupled. The TDR analysis is in the second subfigure as observed in figure 3.37. The first part of the graph to the BO stage is related, then with the vias is continued and that block as the small rise in the graph is represented. The sequence is similar, merely that MR transmission lines are used instead BO until is contacted with the DC-blocking capacitor. This contact is reflected as the last rise before the stimulus ends. As it is observed, one more time the impedance even with all the losses that the model has, it is near to the target impedance.

4 Model Comparison and Analysis

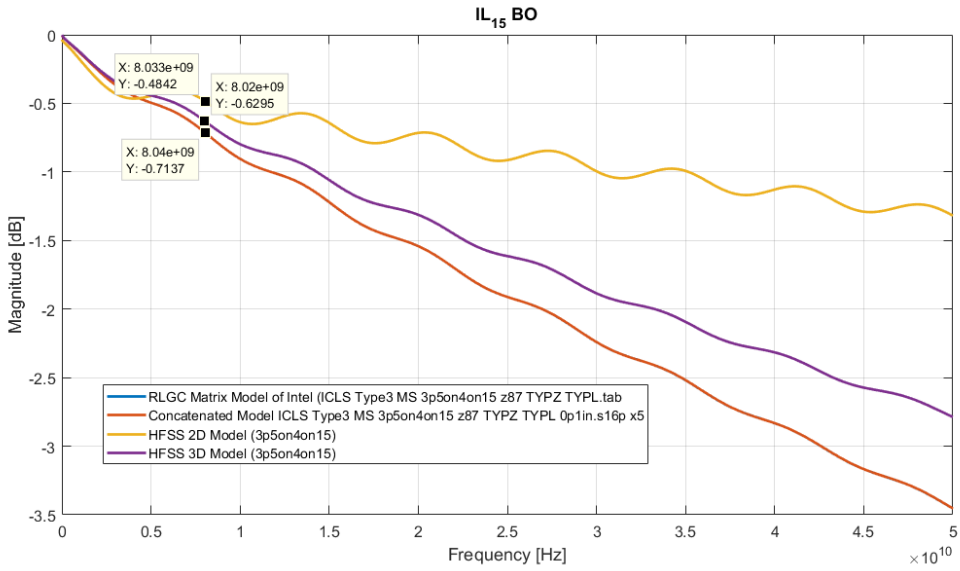
This chapter contains the correlations between the models that in chapter 3 have been built and the models that have been done by different ways and methods as 2D simulators and real measurements. This chapter how much the results between them disagree will show. For this correlation, the S parameters obtained by HFSS simulations and that was provided will be using.

4.1. Transmission Line

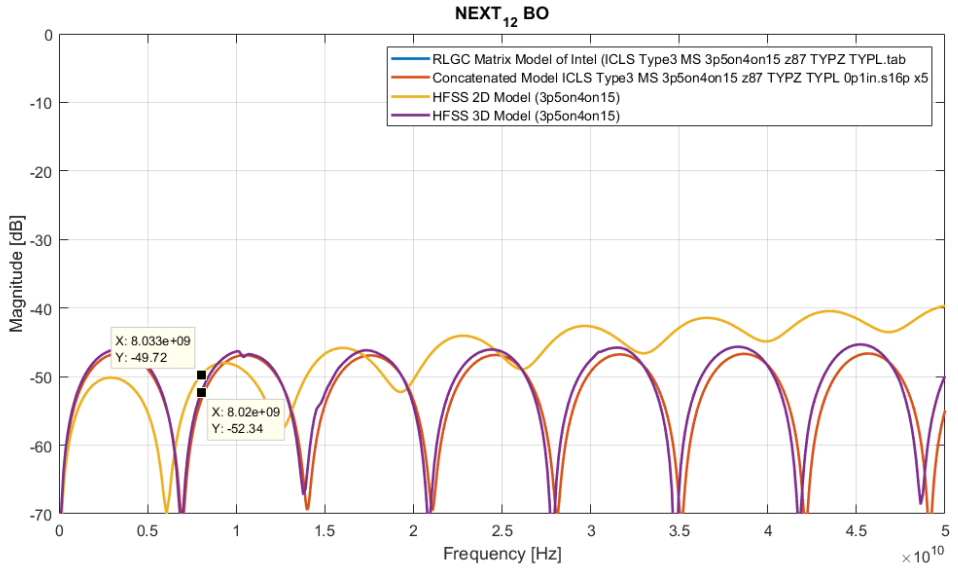
This subsection the results of chapter 3 with results that were provided will be correlated. For this correlation four data will be used. These data are the transmission line obtained by 2D and 3D HFSS simulator, a *.tab* file, which it is a matrix that describes the transmission lines with their *RLGC* elements and the S parameters at a specific length of the line. The advantage of this matrix is that with different lengths and not just one can be configured. This allows flexibility in the manipulation of the S parameters. In figure 4.1 the correlation of the breakout line is observed.



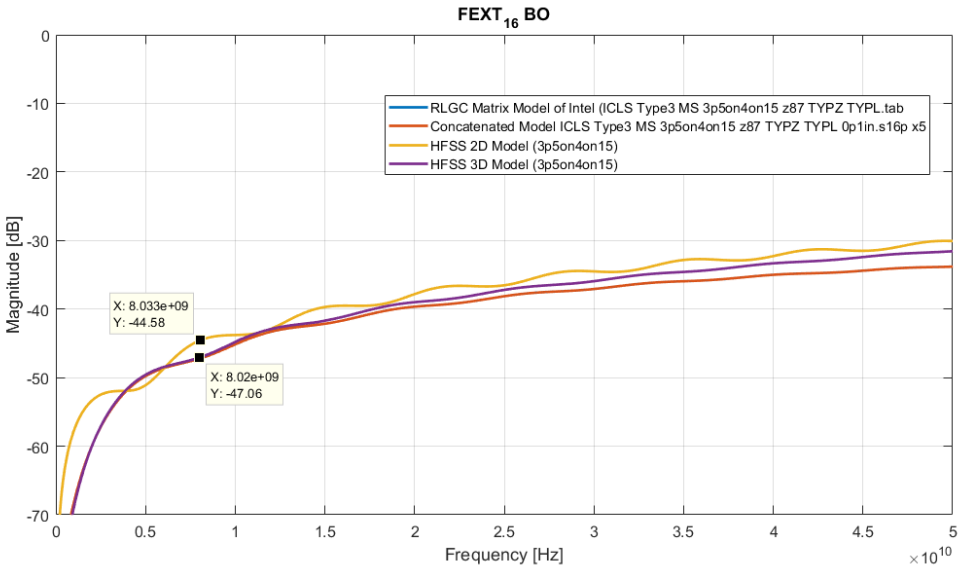
(a) Return Loss of the BO model



(b) Insertion Loss of the BO model



(c) NEXT of the BO model

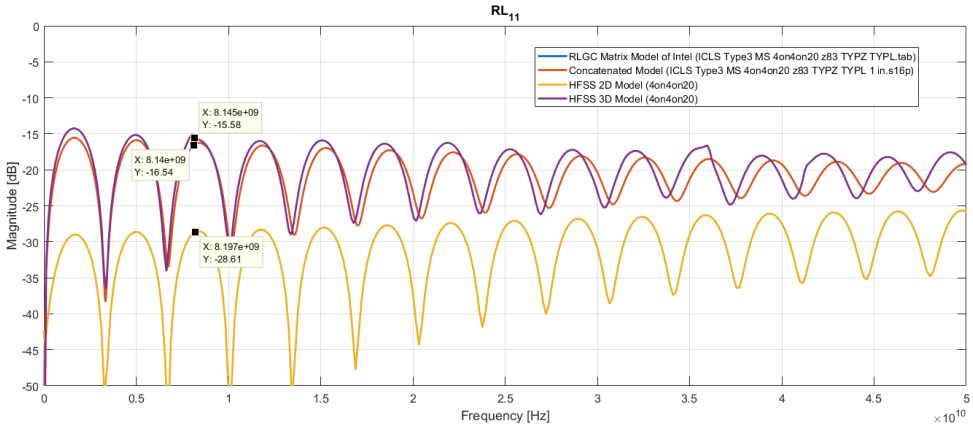


(d) FEXT of the BO model

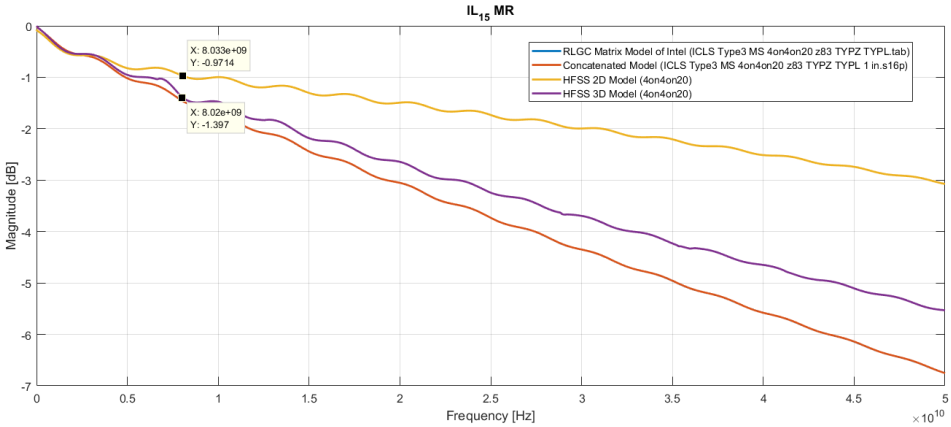
Figure 4.1: Correlation of the transmission line of breakout type

From figure 4.1 can be observed the correlation and the principal characteristics of the provided model for the HFSS 3D model can be captured. The 2D model has some difference respect the others. This is because the solver performs a fast simulation since this lasts 30 minutes or less, while 3D can last a couple of hours. This means that a mesh isn't created as the 3D solver does. Hence, a whole scenario of the line isn't contemplated.

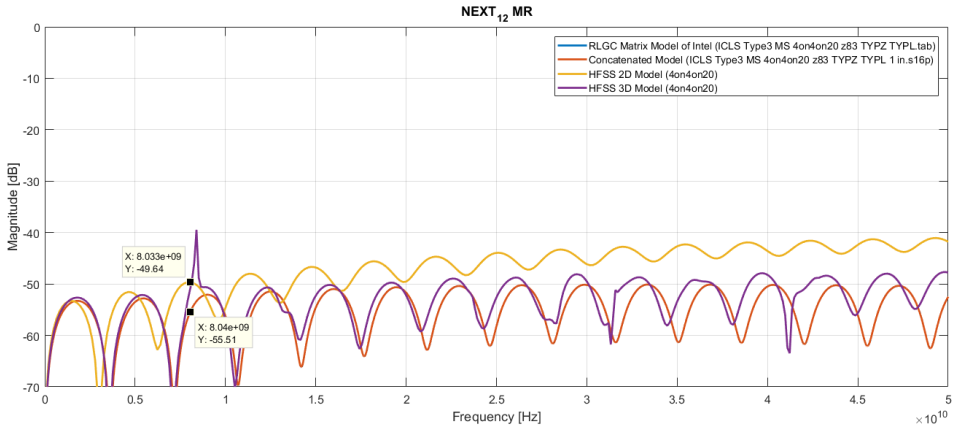
The next correlation is related with the other transmission line, the main route type. As the case of the BO, the same results will be correlated. In figure 4.2 the correlation of the models are shown. At first view the same trend happens as the BO model, merely the 2D differs from the rest of the models. The reason is the model loss that is in use. This introduces an undesirable error, because as was mentioned in this model in chapter 3, a Debye loss model was used and the measures for two frequency points are unknown, just have one data point at 5 GHz.



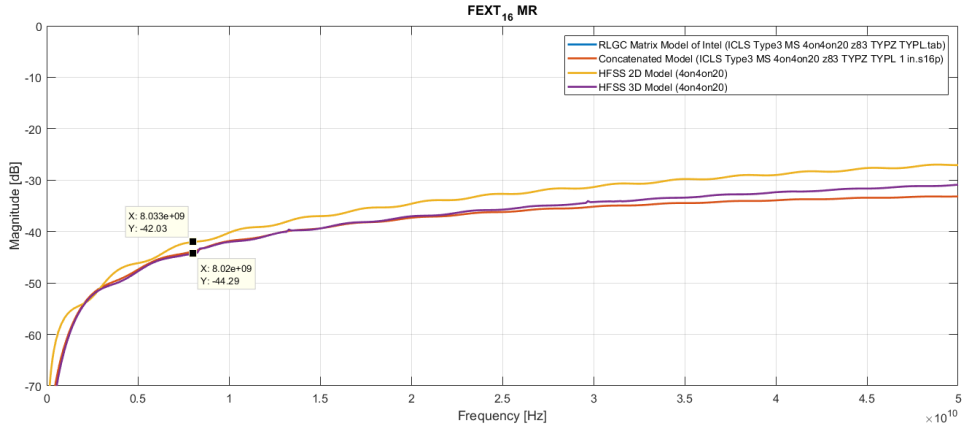
(a) Return Loss of the MR model



(b) Insertion Loss of the MR model



(c) NEXT of the MR model



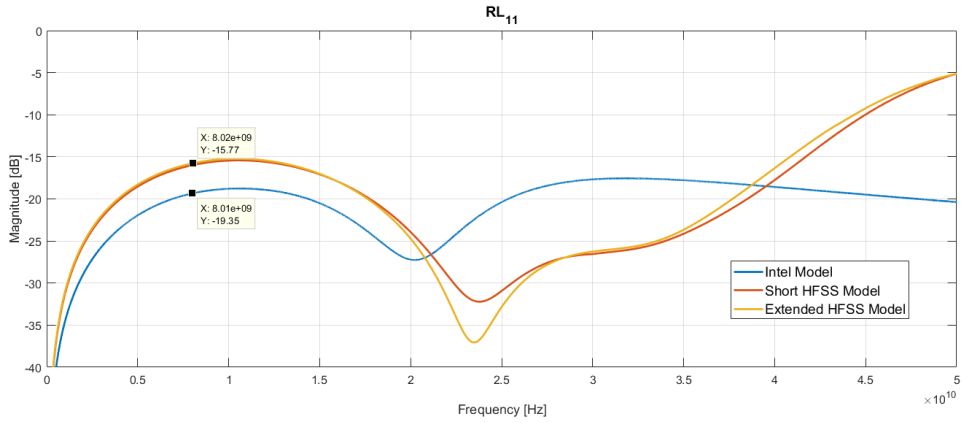
(d) FEXT of the MR model

Figure 4.2: Correlation of the transmission line of main route type

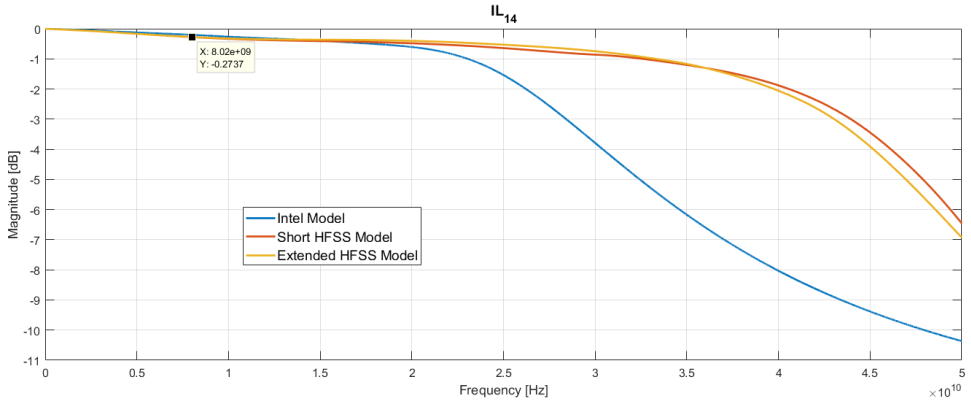
4.2. Vias

The next correlation is related with the via model. The provided model and the model built in HFSS will be correlated. The correlations of these are in figure 4.3. The return loss practically has the same behavior between models. Only the resonance of the provided model it happens before the HFSS models. This occurs because the length of the trace that connects the via wasn't provided. It implies that had to be approximated until it is coincided as much as possible with the resonance of the model of the blue graph.

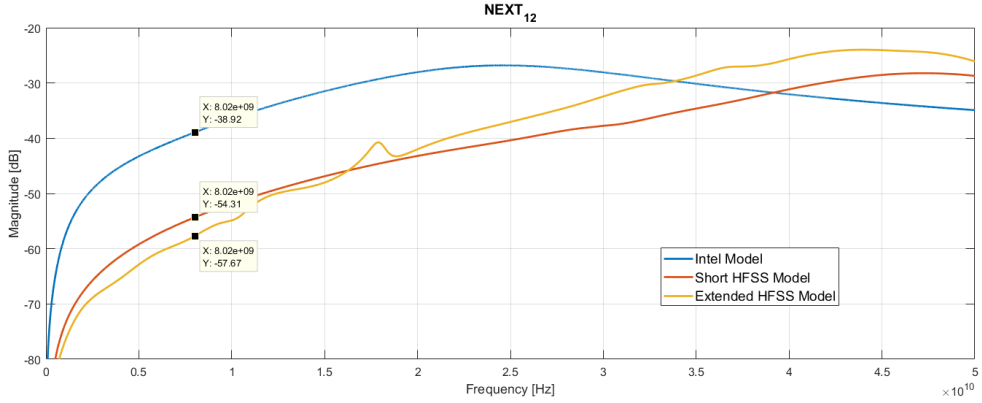
In terms of the transmission can be observed that the HFSS models have a longer bandwidth than the other model. This can be justified with the crosstalk because as observed in the blue graph exist a higher crosstalk. This means that differential pairs are more nearby in the provided model than the differential pairs of the HFSS model. So, in the end, this approach of the pairs generates more losses in the pairs, and this is what happens in the insertion loss graph (subfigure *b*). The errors that exist in the correlation are due to the difference in the trace which connects the port an the via and the spacing between differential pairs.



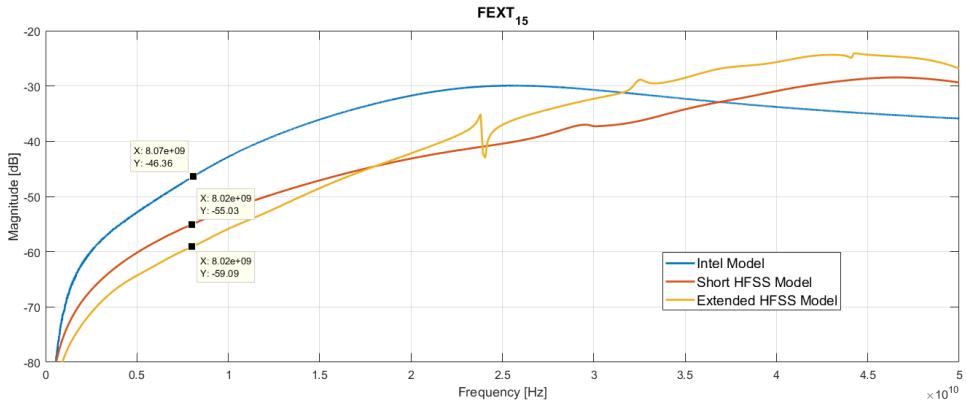
(a) Return Loss of the Via model



(b) Insertion Loss of the Via model



(c) NEXT of the Via model



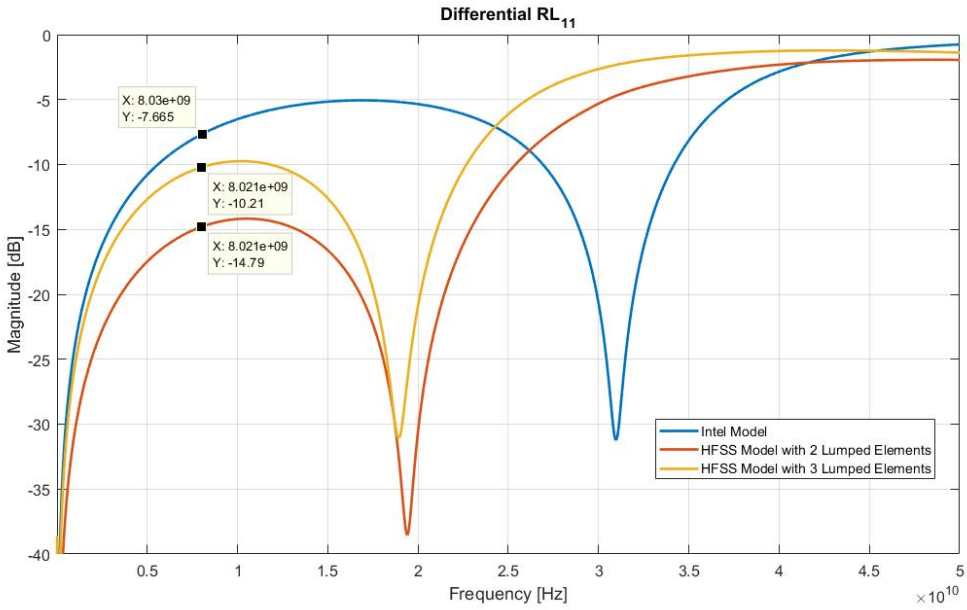
(d) FEXT of the Via model

Figure 4.3: Correlation of the Via model

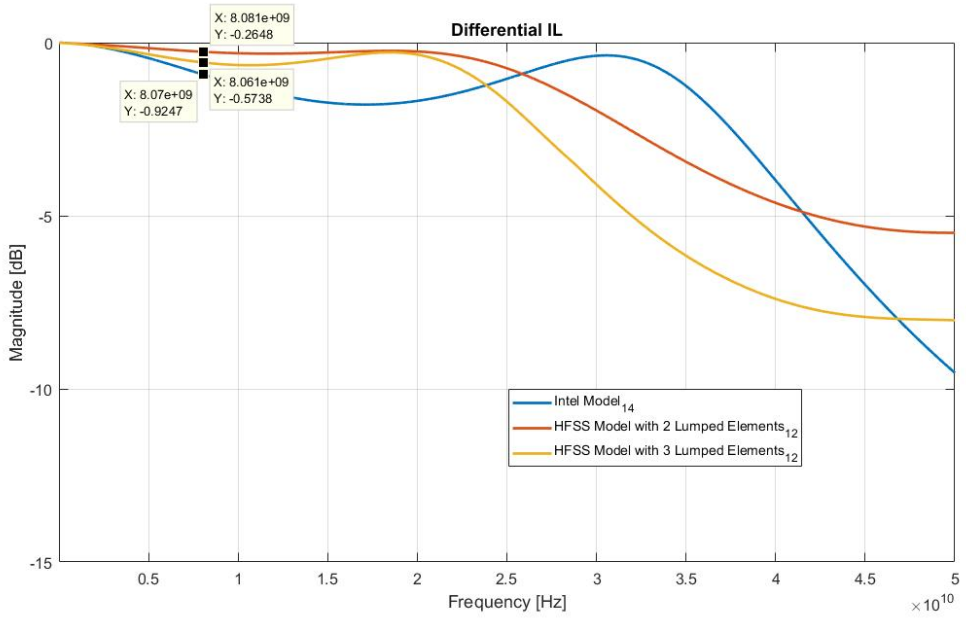
4.3. DC-Blocking Capacitor

This correlation is about the DC-Blocking capacitor. Only the capacitor was modeled. The purpose of this correlation is to see the error that is given by 3D HFSS model in relation with the model that has been obtained by different approaches previously. In figure 4.4 is shown the correlation of three models, which these are the provided capacitor, the HFSS model with resistive and inductive elements (two lumped elements) and the 3D model with capacitive, inductive and resistance elements (three lumped elements).

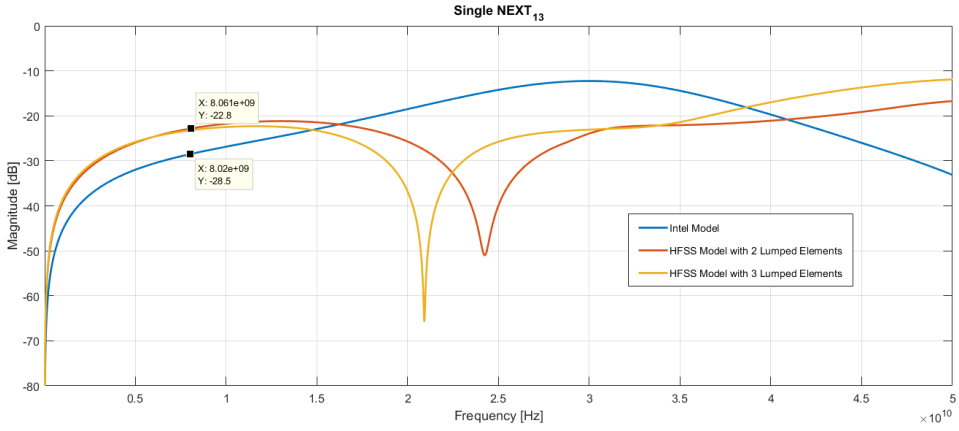
In the correlation a difference between models is displayed. The return loss of the provided model has a minor trace than the 3D model because the resonance in the blue graph is longer respect the others. Besides, blue graph is the model that has more losses, because the reflection is -7.665 dB and the other models are below of -10 dB. In terms of transmission, the provided model has more transmission bandwidth but also has an abrupt decrease since 30 GHz. The crosstalk only in single mode can be analyzed because just one differential pair was modeled. In NEXT and FEXT can be observed, that the single lines don't influence in the others.



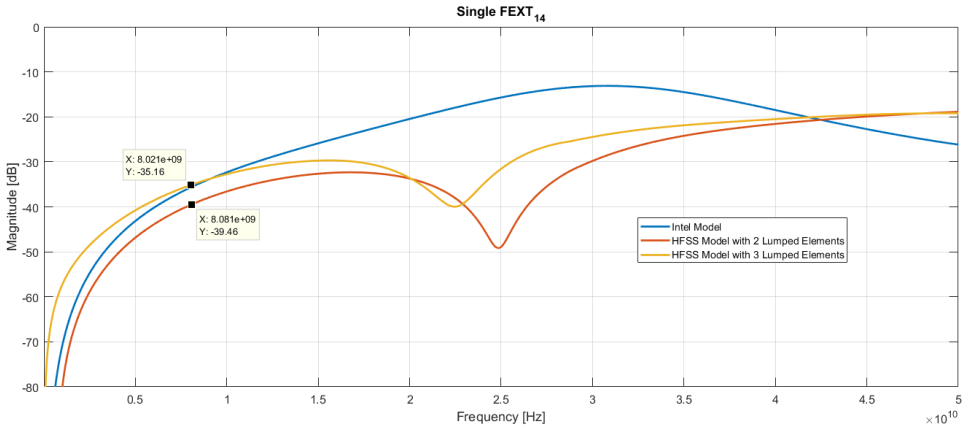
(a) Return Loss of the DC-Blocking capacitor model



(b) Insertion Loss of the DC-Blocking capacitor model



(c) Single NEXT of the DC-Blocking capacitor model



(d) Single FEXT of the DC-Blocking capacitor model

Figure 4.4: Correlation of the DC-Blocking Capacitor

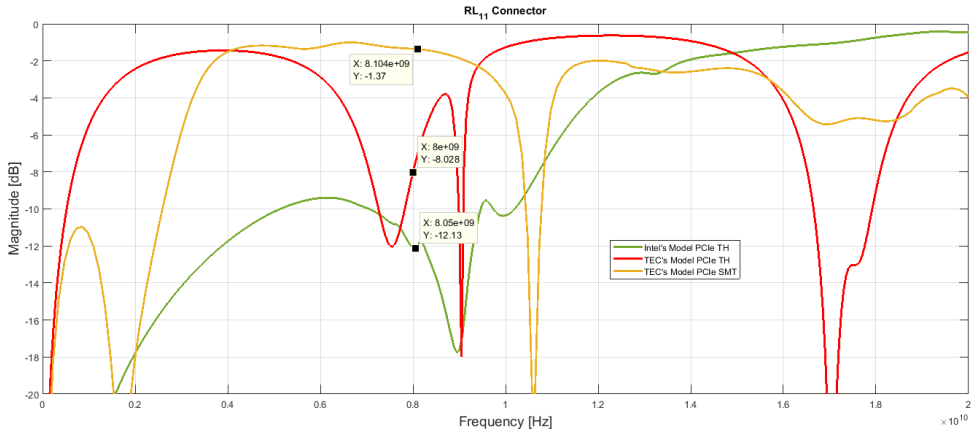
In summary of this correlation, several things can be observed and these are:

- The provided model is the model with most losses.
- The length trace of the provided model is less than the HFSS models.
- The inclusion of third lumped (capacitive) element in the HFSS model, produces more losses and a reduction of the transmission.

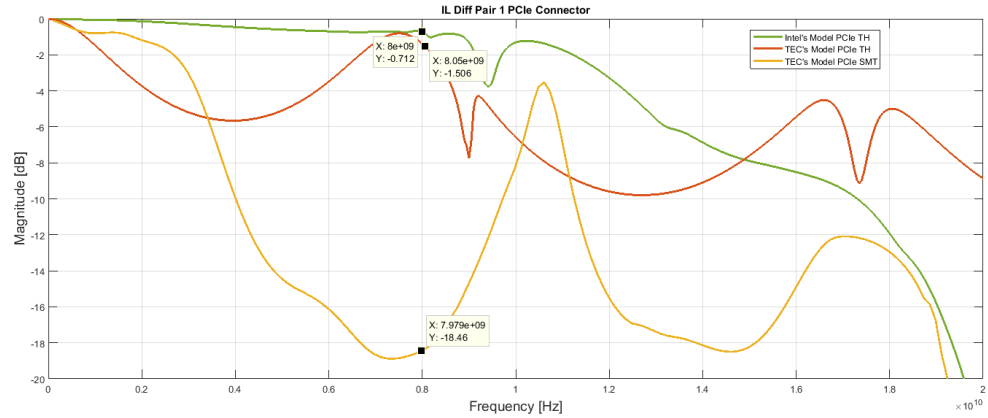
4.4. PCIe Connector

This section contains the correlation of the PCIe connector. This is done to observe the behavior of the connector that PCIe buses use, and see how much is the error of the

connector built in chapter 3. In figure 4.5 is observed the correlation of the PCIe connector. The transmission of the connector provided has a loss of -3 dB up to in 10 GHz, while the rest of the models are in less than 3 GHz. The possible reasons are the differences the ports assignment as well as the pins assignment. In chapter 3 different models were realized and neither at the fundamental frequency could operate. Finally, the environment in how the correct connector was simulated is unknown, so this implies work blind for the sake to get the best correlation.



(a) Return Loss of the PCIe connector model



(b) Insertion Loss of the PCIe connector model

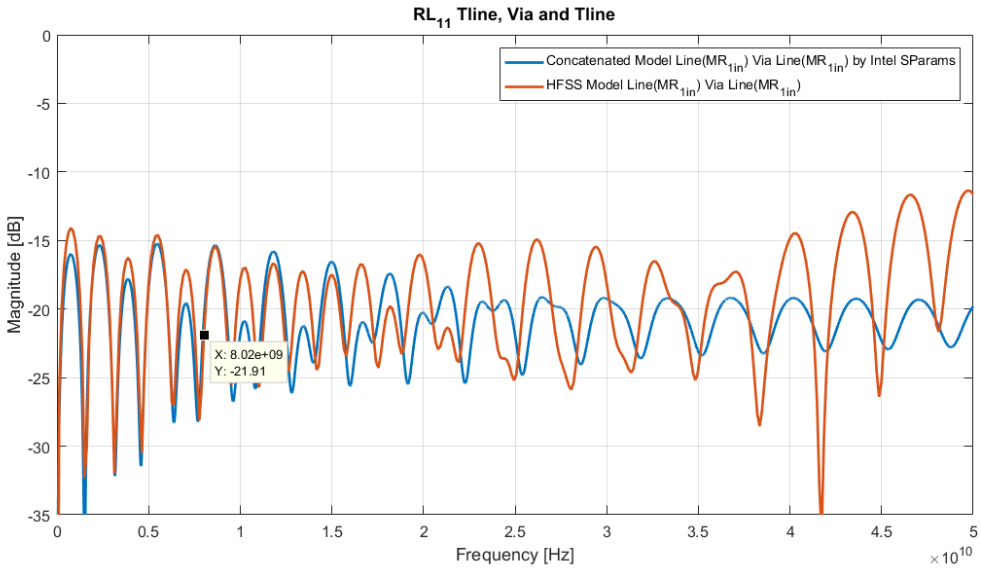
Figure 4.5: Correlation of the PCIe Connector

4.5. Transmission Line and Via

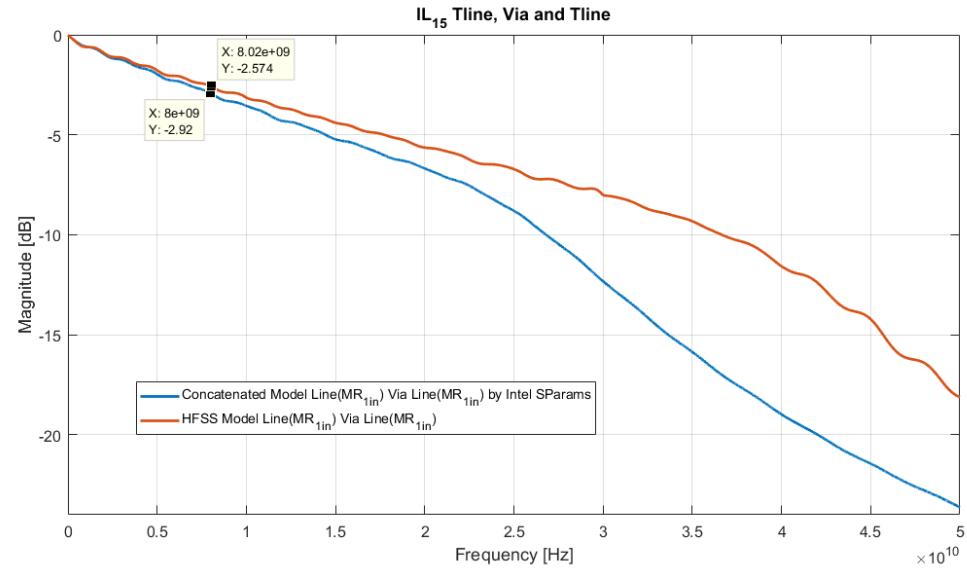
To verify the results of the models concatenated, it will be correlated the concatenated model already supplied and concatenated models with the lengths of the basic models. In figure 4.6 is observed the correlation of the model, which contain transmission lines and vias. At first view in the return loss is obtained the same behavior for both models up to

a frequency of 15 GHz approximately. The inclusion of the vias, cause differences between models. Until the fundamental frequency, the models almost have the same response. The correlation is complying due to the models are similar between them, since the difference in terms of magnitude is less than -3 dB. Also, in the insertion loss is shown a similar response until a frequency of 20 GHz where the difference between models is less than -1 dB. After that is can be observed that HFSS model has fewer losses but considerable.

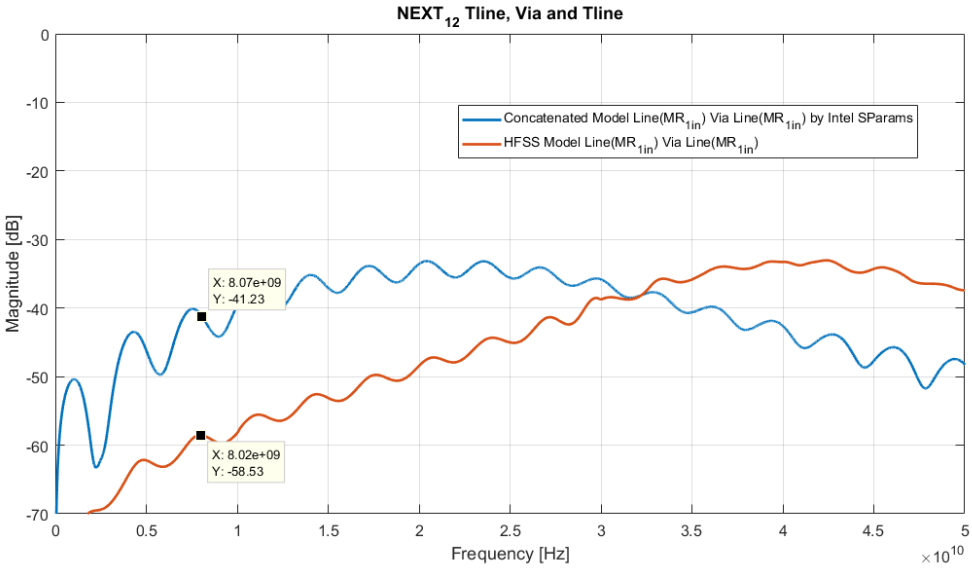
With the crosstalk is noted, the same situation as in the via correlation because the crosstalk is higher for the provided model than the HFSS model. This reason implies the increase in losses for the model that were provided. Besides, the differential pairs are more nearby than in the HFSS model.



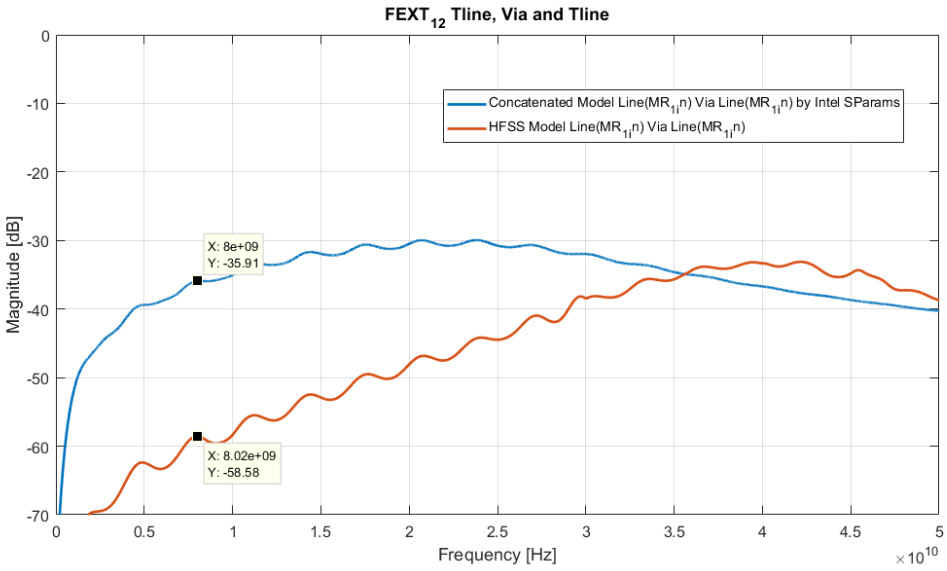
(a) Return Loss of the TL, Via and Tl model



(b) Insertion Loss of the TL, Via and TL model



(c) NEXT of the TL, Via and TL model



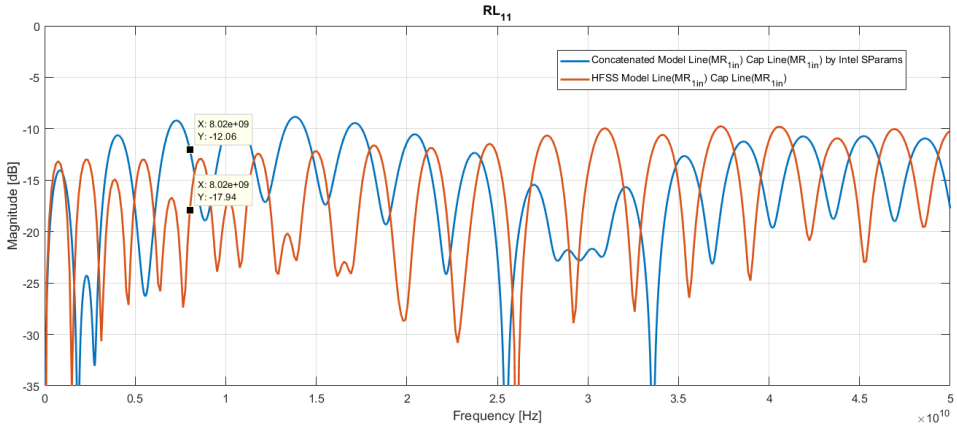
(d) FEXT of the TL, Via and TL model

Figure 4.6: Correlation of the TL, Via and TL model

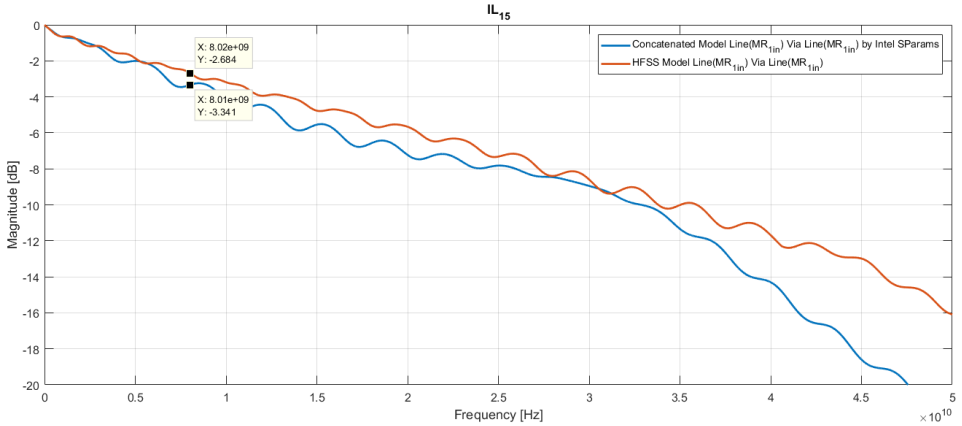
4.6. Transmission Line and DC-Blocking Capacitor

In this section the concatenation of the transmission line and DC-blocking capacitor is correlated. The results of the correlation can be observed in figure 4.7. The blue graph is the provided model and the red one is the model simulated in HFSS. With the return loss can be observed that the models correlate up to 2 GHz. There are differences between the models, as in the capacitor model, the track length between capacitors differs. This induces differences that are observed as frequency shifts in the graphs of the models. It's observed that the configuration of the model provided includes more losses than the 3D model.

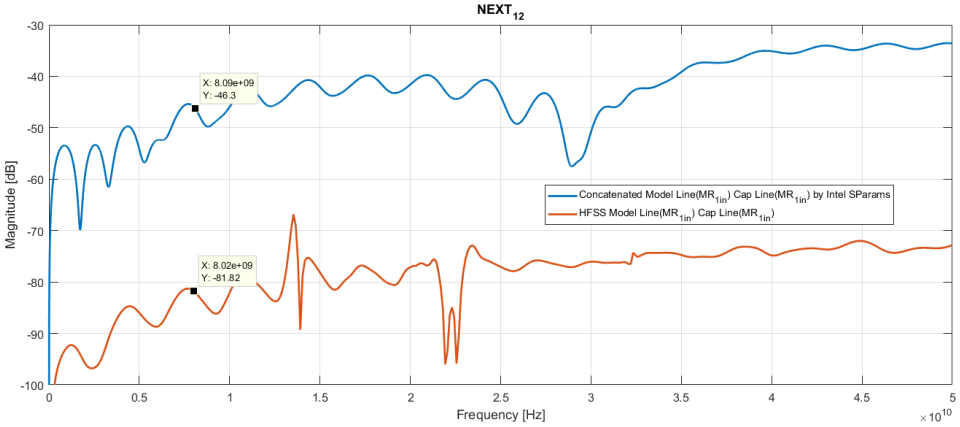
It is correlated the insertion loss since among them there is less than 1 dB of difference. In high frequency, the blue graph presents more losses and is by the configuration of the capacitor of the provided model. The crosstalk in both models has the same trend. The problem is in the spacing that exists between differential pairs since is not the same for both models. Even, the crosstalk wouldn't affect the transmission as the capacitors do.



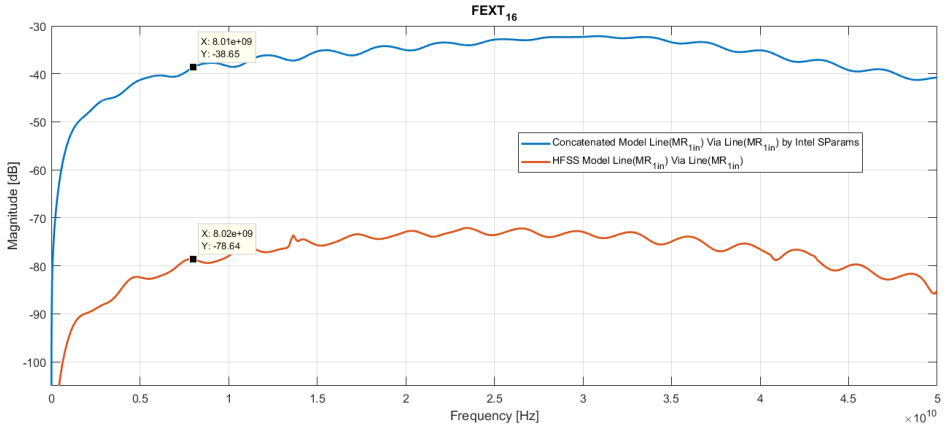
(a) Return Loss of the TL, Capacitor and TL model



(b) Insertion Loss of the TL, Capacitor and TL model



(c) NEXT of the TL, Capacitor and TL model



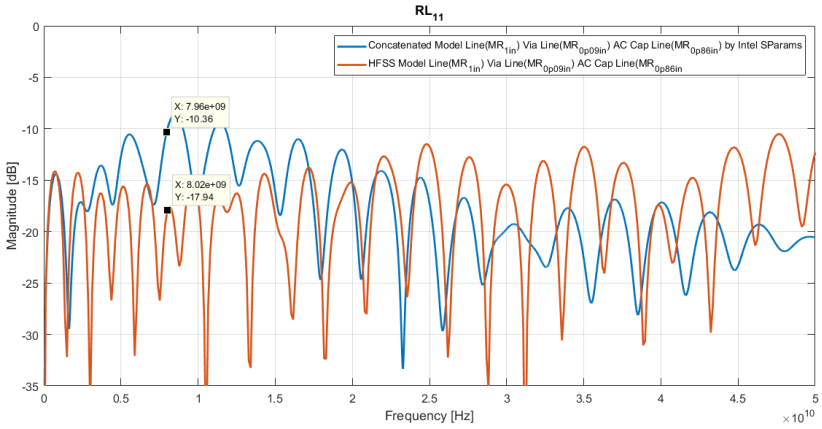
(d) FEXT of the TL, Capacitor and TL model

Figure 4.7: Correlation of the TL, Capacitor and TL model

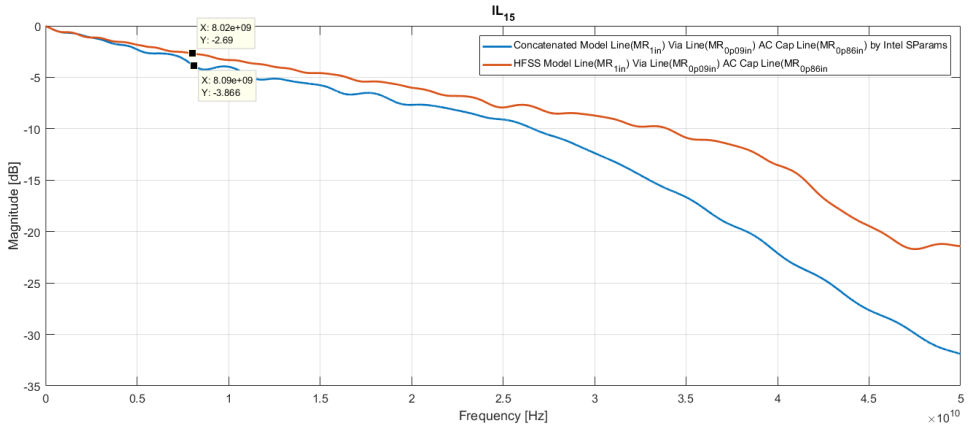
4.7. Transmission line, Via and DC-Blocking Capacitor

This correlation is related to the concatenation of models as transmission lines, vias, and DC-Blocking capacitors. In figure 4.8 the correlation of the models are observed. The return loss starts to have difference since 5 GHz, but this model has the same reasons of previous models that contain the capacitor. Even, the correlation in most of the sweep, the difference in magnitude is less than 5 dB. Something interesting to see is the resonances because the resonances of the 3D model are more than provided model. It means that the provided model, has less length than the HFSS model, and this could be by the length of the capacitors and the vias.

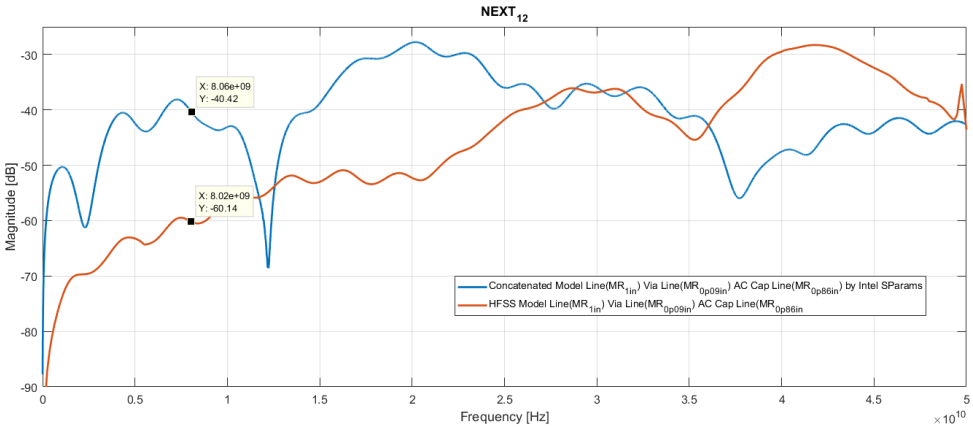
The transmission is modeled by the insertion loss and can be observed that exists 1 dB of difference between models until a frequency of 25 GHz. Later, the losses of the capacitor of the provided model cause the transmission of the same model falls quickly and also the length of the transmission lines. While the HFSS's model falls in a softer way. Finally, the crosstalk doesn't correlate due to the spacing between differential pairs that are different for both models but has some trend trough the frequency sweep.



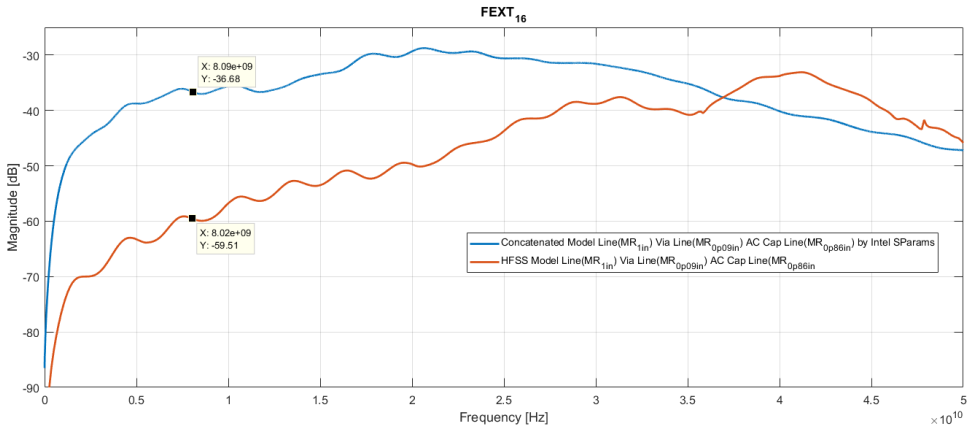
(a) Return Loss of the TL, Via, TL, Capacitor and TL model



(b) Insertion Loss of the TL, Via, TL, Capacitor and TL model



(c) NEXT of the TL, Via, TL, Capacitor and TL model

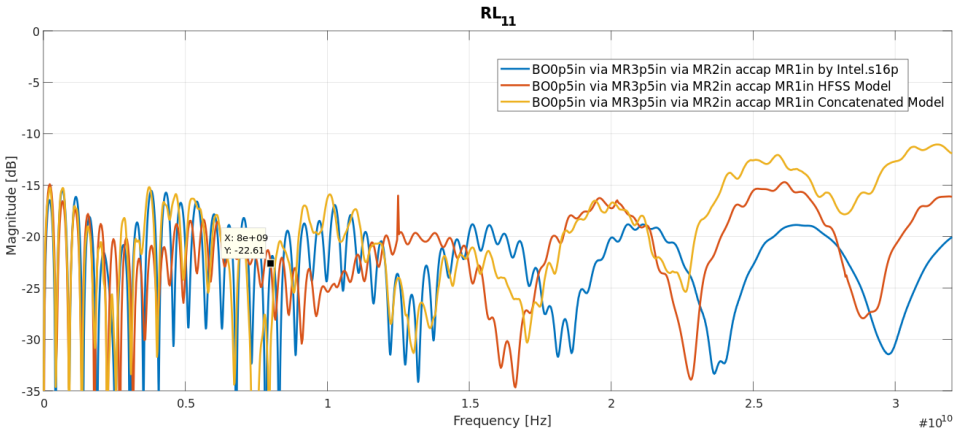


(d) FEXT of the TL, Via, TL, Capacitor and TL model

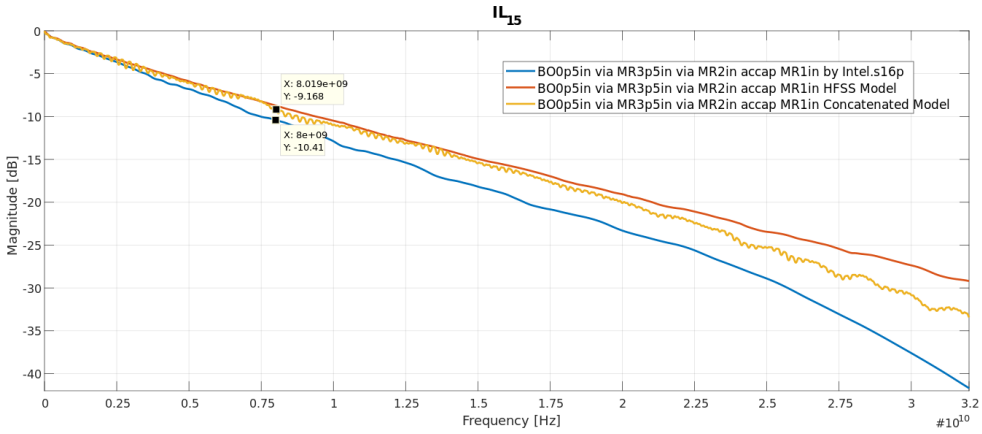
Figure 4.8: Correlation of the TL, Via, TL, Capacitor and TL model

4.8. Full PCB Path

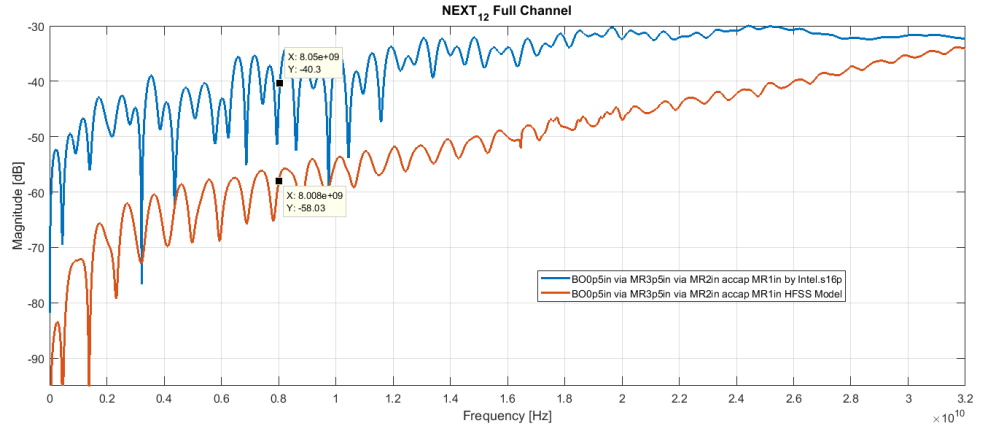
The final model that will be correlated is the concatenation of all the elements except the PCIe connector. This includes the transmission lines (BO and MR types), vias and capacitors. This channel is connected from the motherboard exit until the entry of the connector. In figure 4.9 the correlation of the channels can be observed. There are three graphs, the blue graph is the provided model, the red graph is the full 3D model and the yellow graph is the concatenation of the single models validated in HFSS. The third graph only with the return and insertion loss is correlated because are parameters that only have two ports.



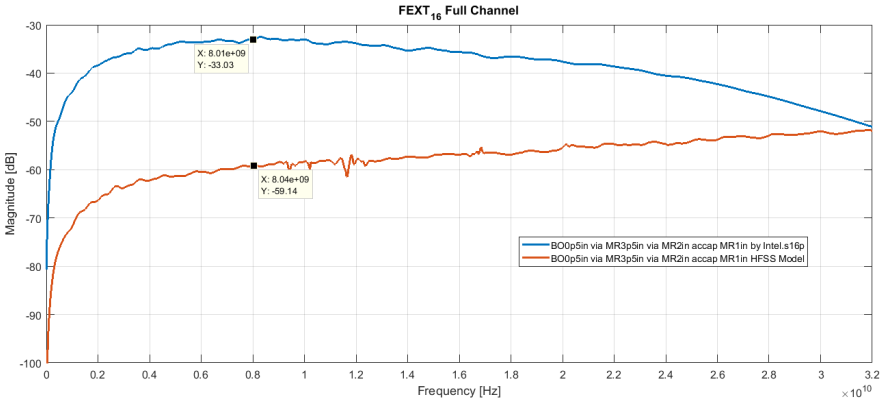
(a) Return Loss of the TL, Via, TL, Capacitor and TL model



(b) Insertion Loss of the TL, Via, TL, Capacitor and TL model



(c) NEXT of the TL, Via, TL, Capacitor and TL model



(d) FEXT of the TL, Via, TL, Capacitor and TL model

Figure 4.9: Correlation of the Full PCB Path Model

The return loss that is shown in figure 4.9, has a difference between 2 and 3 dB until a frequency of 12 GHz between models. After that, the blue and yellow graph is kept nearby until 15 GHz. Since that frequency, all the models differ between them due to the differences in the definitions of the models in terms of length.

The transmission is given by the insertion loss and the same situation as in previous models is shown, where in the provided model more losses than the HFSS models is presented. The reason of that is the length of the channel. As the line grows, more losses will be generated. In this model the length is of seven inches. Respect to other models, this is the longest channel and as it is observed, it is the channel with more losses. For the crosstalk is observed, NEXT and FEXT have each one, almost the same response but a huge difference in magnitude. This occur due to the spacing of the differential pairs which are not the same.

In summary, the concatenation of the single models, also provide an approach that show a very small variation up to 20 GHz with respect to the full 3D model. The advantage is that could be avoid the use of a huge quantity of computational resources.

4.9. Simulation Time

As a final comparison the simulation times obtained are shown. The used resources came from TEC and Intel. The simulation times of the basics models and the concatenation are detailed in table 4.1. In this table is observed, the single models with the TEC's resources took a lot of time in comparison with the Intel's resources with the case of the full PCB path. These times indicate how much is the simulation time to model a three dimensional geometry. As shown, either TEC's or Intel's resources, the time to obtain a result is considerable in comparison with a 2D simulation that takes just some minutes. With the obtained results, can be said that the different approaches that were provided, it is still a good option to avoid the use of great computational resources.

Table 4.1: Simulation comparison by different resources

Model	**TEC**			**Intel**		
	Real time	CPU Time	Memory (GB)	Real time	CPU Time	Memory (GB)
TL (BO and MR)	10h / 13h	9.5h / 13h	2.17 / 6.81	2h / 3∼4 h	——	——
Via	2h	2h	0.923	——	——	——
DC-blocking Capacitor	20 min	10min	0.025	——	——	——
PCIe connector	59h	36h	4.39	——	——	——
Full PCB Path	——	——	——	12h	——	——

Furthermore, the CPU time and the memory consumption are detailed in table 4.1. The details of the Intel's simulations cannot be obtained because they are that to processing are dedicated. These resources uses parallelism by code from console, so details as the shown in table 4.1 cannot be extracted, just the results of S parameters and the mathematical solution of the project.

On the other hand, the same details from the TEC's resources can be obtained, as it works with the graphical interface. These are shown in the table 4.1. The times between CPU and real are observed to be approximately the same. There is a difference in the times of the connector model, due to the complexity of the meshing process. But this complexity does not imply more memory use, since more memory for the lines than for the connector is used. Therefore, it is shown that different variables must be taken into consideration for the modeling of three dimensional geometries, which may be simple in meshing but complex in length and solution in frequency. Whereas the opposite may occur, as well as having a complex meshing with great length and an extensive solution in frequency, i.e. to analyze beyond the fundamental frequency.

5 Conclusions and Recommendations

Models for a PCIe bus were created and evaluated, complying with the mechanical characteristics and electrical specifications. It is shown that these models might work for the PCIe 4.0 that operates with a fundamental frequency of 8 GHz. From the obtained results, with the studied topology, its observed that the transmission lines are the components inserting more loss at lower frequencies, however vias and DC-blocking capacitors introduce a step loss at higher frequencies.

It was possible to correlate the results that were obtained from the three dimensional models and the segmented models, where most of the cases correlated with an error of 3dB or less for the insertion loss and less than 5 dB for the return loss at the frequency of 8 GHz. For those that do not approximate very well, a cause attributed to the model definition was found.

Considering only signal paths, the segmented approach provided good results up to 20 GHz, whereas deviations at higher frequencies could be observed. As expected, the segmented approach is more efficient in terms of computation time and computational resources. In summary, it is concluded that segmented models can still be used in that frequency range since the correlation shows that there is no significant difference. For frequencies beyond 20 GHz, a more detailed evaluation of the models is recommended, which might also include power noise effects.

Various recommendations for this work exist. The analysis could be extended to a combined power and signal integrity analysis, where the interactions of the signal and power domain could be mapped. This type of analysis could be also improved by including hardware measurements and the corresponding model-to-hardware correlation.

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