A WDM 4x28Gbps Integrated Silicon Photonic Transmitter driven by 32nm CMOS driver ICs

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Abstract: A four-channel WDM silicon photonic transmitter with integrated lasers and modulators driven by low-power 32nm CMOS drivers, is demonstrated to operate at a data rate of 4×28Gb/s with BER<10^{-12} and power consumption of 10.0pJ/bit.
OCIS codes: (200.4650) Optical interconnects; (250.5300) Photonic integrated circuits

1. Introduction

There is a growing demand in datacenters for low cost, high bandwidth, single-mode optical transceivers that have reaches up to 10km. Concurrently, there is a strong push to reduce the power consumption of these links, especially, when trying to reach the bandwidth targets of next generation standards, such as 400GbE [1]. This requires solutions that scale efficiently with data rate and channel count. Furthermore, to meet power and cost targets it is necessary to move photonics out of hermetically sealed "gold box" packages and into ones that more closely resemble electronics in order to realize the cost advantages and advanced packaging capabilities developed for the electronics industry.

In practice, the combination of WDM-capability with electronic-like packaging is challenging. Conventional III-V semiconductor based photonic transceivers enable WDM performance but fall short on power consumption and cost due to the limitations of "gold box" packaging. In contrast, typical silicon photonic transceivers enable low power and cost solutions for a small number of wavelength lanes but have failed to enable WDM scaling to high channel count, limited in transmitter architectures by the use of external lasers that are inefficient and require assembly processes to scale [2,3], lasers with coarsely-spaced wavelengths that quickly exceed the fiber window [4], or relatively inefficient C-band lasers that lead to high energy per bit for each channel [3,5,6].

In this work, we demonstrate a four-channel implementation of a WDM photonic transmitter technology driven by CMOS electronics, with extremely low 10.0 pJ/bit wall-plug power consumption (not including thermo-electric cooler). As depicted in Fig.1, by virtue of integrating lasers, modulators and MUX components onto a single chip and closely integrating it with low power CMOS drivers via advanced packaging, this WDM photonic transmitter can scale to higher channels counts while staying within the power and cost envelope required by data centers.

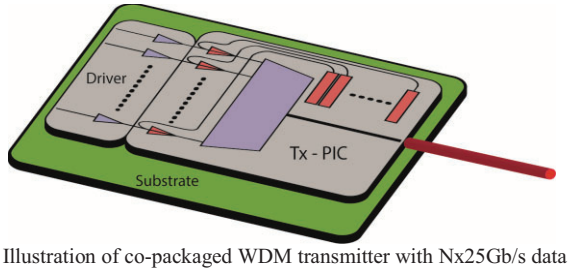

Fig. 1: Illustration of co-packaged WDM transmitter with Nx25Gb/s data paths.

2. Photonic integrated circuit and driver circuit details

The photonic integrated circuit (PIC) demonstrated in this work consists of four tunable lasers [7], which are individually coupled to four electro-absorption modulators (EAMs). The outputs of the EAMs are multiplexed on the PIC via Multi-Mode Interference (MMI) combiners. The lasers and EAMs on the PIC were fabricated simultaneously using Aurrion's heterogeneous integration process. Fig. 2 (a) shows the output optical spectrum of the PIC (including fiber coupling losses) where the wavelengths of the lasers have been tuned to match the 100GBASE-LR4 grid. If required, they can be tuned to a narrower channel spacing, for example, 200GHz, in order

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to maximize spectral efficiency especially when scaling to higher channel counts. Fig. 2(b) shows the absorption curves of the EAM. The EAM epitaxial layer designs are similar to those reported in [8] and can support an optical bandwidth of ~30nm.

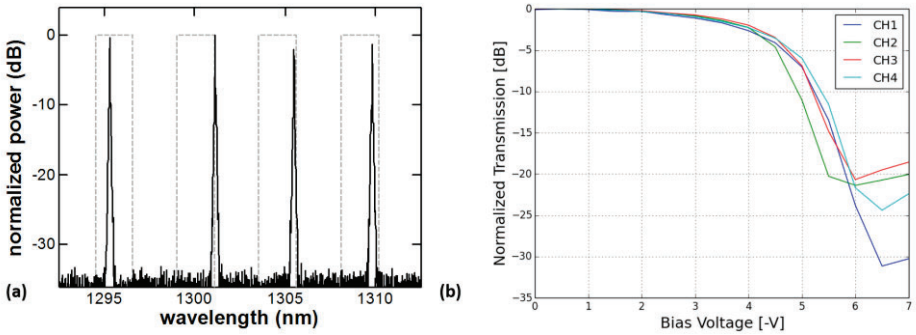

Fig. 2: (a) measured output spectrum for the four transmitter channels where the wavelengths have been tuned to 1295.3, 1301.1, 1305.5 and 1309.8nm, respectively. (b) Normalized transmission of the EAMs on the PIC as measured using an on-chip tap detector.

The driver integrated circuit (IC) is fabricated in IBM's 32nm SOI CMOS technology and its details have been reported in [8]. The driver provides $2V_{p\text{-}p}$ output swing per channel and dissipates an overall power of 97.6 mW when the transmitter is operating at 4 x 28Gbps. The lasers and EAMs contribute 1004mW and 18.5mW, respectively. Along with the CMOS driver, this results in an overall transmitter power consumption of 10.0pJ/bit. It should be noted that unlike in [3], where the output stage RLC network of the driver was optimized to match the design of the EAM array, the EAMs on this PIC were not co-designed with the driver and this in turn limited the performance of an individual channel to 28Gbps compared to 32Gbps reported in [9].

3. Measurements and Results

The PIC was wire-bond packaged on a custom printed circuit board with four single-channel driver ICs (see Fig. 3). Supply voltages and current biases were delivered through ribbon cables while four high-speed differential-pair inputs were routed through MMPX connectors at the card edge across micro-strip transmission lines and terminated into 100-Ω differential input terminations in each of the driver ICs. Fig. 3 shows a block diagram of the experimental setup. An Anritsu MP1800A pattern generator (PG) configured with 2 dual-channel MU183020A modules was used to simultaneously provide four decorrelated 28Gbps signals encoded with a PRBS pattern of length 2^{31}–1 to the card. A thermo-electric cooler was used to hold the card at 32°C to maintain test setup stability for this power measurement. However, the PIC is capable of operating at significantly higher temperatures, and each laser can be held at a constant wavelength even as the temperature changes with appropriate tuning.

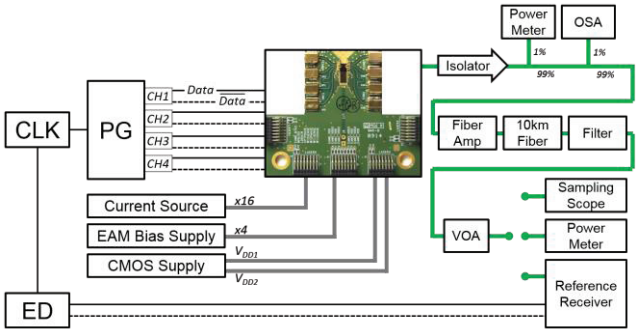

Fig. 3: Block diagram of experimental setup with photograph of the packaged assembly.

Light was extracted from the PIC using a single-mode tapered-lensed fiber with an approximate 2.5μm spot diameter. The light was then passed through an isolator, a praseodymium-doped fiber amplifier, a 10-km spool of single-mode fiber, a tunable Fabry-Perot filter, and a variable optical attenuator (VOA). Finally, an optical switch was used to select between a sampling scope with a 30-GHz photodetector plugin, an optical average power meter, or a reference receiver (RX). The RX consists of a custom 130-nm SiGe IC wire-bonded to a photodetector with 0.6A/W responsivity at 1310nm. The RX's differential outputs were connected to an error detector (ED). The transmitter was tested with all channels running simultaneously, filtering out one at a time on the RX.

The captured eye diagrams are included in Fig. 4(a) for all four channels at 28 Gbps per channel. Although extinction ratios up to 10dB have been demonstrated using similar drivers with similar EAMs [9], in this case the EAM biases were set to provide smaller extinction ratios of 5.9dB, 5.5dB, 6.6dB, and 7.0dB in order to increase the optical modulation amplitude. The observed noise and jitter present in the eye diagrams is an artifact of the aforementioned independent design efforts, and has been shown to be significantly improved with co-design [9]. Bit error rate (BER) curves were recorded for all four channels, first back-to-back (B2B) and then through the 10km fiber. The BER curves are plotted in Fig. 4(b) against average optical power, corrected to infinite extinction ratio. The curves for the four channels exhibit a spread of about 2dB at a BER of 10^{-12}, attributed to variations in package parasitics. Furthermore, the curves indicate no measured power penalty through the fiber for all four channels.

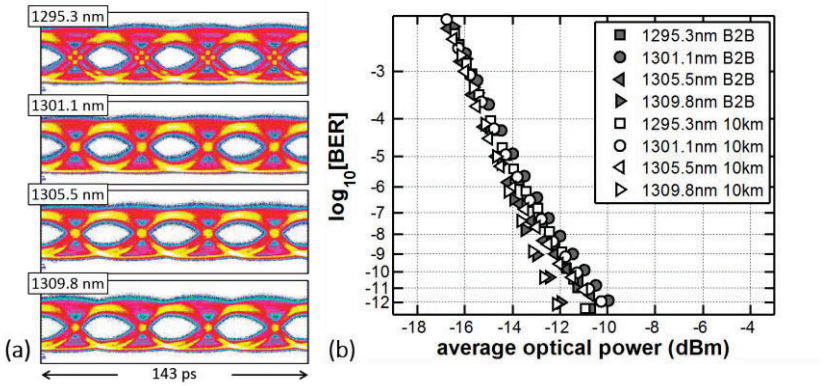

Fig. 4: (a) Eye diagrams for the four channels at 28 Gbps per channel after 10km of fiber propagation. (b) BER curves for the four channels before and after fiber propagation.

4. Conclusion

A 4x28Gbps WDM silicon photonic transmitter with 10.0pJ/bit power consumption was demonstrated. This result shows the promise of this WDM silicon photonic transmitter technology and bears testament to the potential of delivering on low power, low cost, high-channel-count WDM transceivers.

5. Acknowledgment

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