A WDM-Compatible 4 × 32-Gb/s CMOS-Driven Electro-Absorption Modulator Array

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Abstract: A four-channel electro-absorption-modulator array, driven by 32-nm CMOS drivers providing 2-V peak-to-peak output swing, operates with BER < 10^{-12} at a data rate of 4 × 32 Gb/s and dissipates 170 mW of power.

OCIS codes: (130.4110) Integrated optics modulators; (200.4650) Optical interconnects.

1. Introduction

High-bandwidth, energy efficient, and low cost optical transceivers are needed to meet the ever-growing demands of high-performance computing and datacenter networks. Reaching the aggressive bandwidth targets outlined in next-generation standards, such as 400 Gb/s Ethernet [1], requires significant improvements over current commercial technologies, and is more easily achieved when scaling both data rate and channel count. In this work, we investigate the potential of high-channel-count transmitters by assembling and characterizing an array of densely integrated silicon photonic modulators with an array of low-power CMOS drivers. Four-channel modulator and driver arrays are co-designed, co-packaged, and demonstrated operating with an aggregate bandwidth of 128 Gb/s and a combined power consumption of 170 mW. Previously, four-channel silicon photonic transmitters have been reported up to 27 Gb/s per channel [2,3]. Here, the density and efficiency afforded by advanced CMOS electronics and heterogeneously integrated III-V/Si photonics provide promise for scaling channel counts in the future while maintaining aggressive cost and power targets. Furthermore, heterogeneous integration enables the combination of lasers, modulators, and detectors in a single chip, promising future high-channel-count transceivers [4].

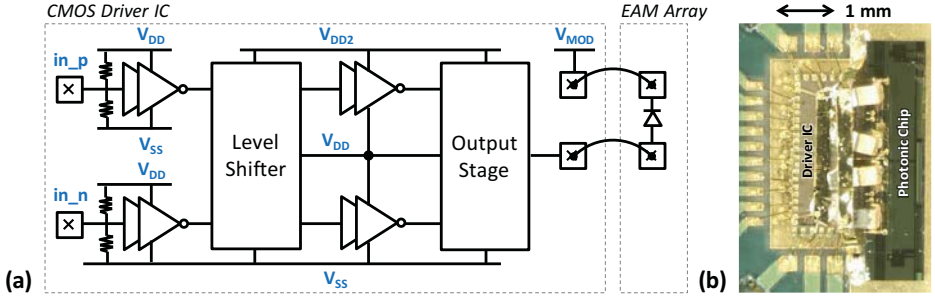

Fig. 1: (a) Electrical drive circuit block diagram for one channel within the array. (b) Photograph of the wire-bond assembly.

2. Details of the Driver Circuits and Modulator Array

The driver integrated circuit (IC) was fabricated in IBM's 32nm SOI CMOS technology. It has a similar architecture to the single-channel driver reported in [5], but modified for lower power and to achieve a better interface with the modulator. Fig. 1(a) depicts the block diagram for one channel of the four-channel driver. Each channel receives differential electrical inputs (*in_p* and *in_n*) into on-chip 50-Ω terminations, which in turn drive a first stage of cross-coupled CMOS inverters that amplify the signal to swing from V_{SS} to V_{DD}. Subsequently, the level shifter provides two outputs swinging from V_{SS} to V_{DD} and from V_{DD} to V_{DD2}. These outputs drive a single stacked CMOS inverter chain. The cascode output stage limits the static voltage across any device to V_{DD} while providing output swing of V_{SS} to V_{DD2} [6]. The driver output connects to the anode of the electro-absorption modulator (EAM), while significant decoupling is applied to the cathode supply (V_{MOD}). Fig. 1(b) shows a micrograph of the module. The pad-limited driver IC measures 1.0 mm × 2.7 mm, while each channel's core circuits occupy 20 µm × 100 µm.

The modulator array was fabricated with Aurrion's heterogeneous integration process. The chip consists of four edge-coupled, 150-µm-long, III-V EAM devices heterogeneously integrated with silicon waveguides. The EAM designs are similar to those reported in [5]. The devices operate over a large wavelength range of approximately 30 nm, provide an extinction ratio (ER) larger than 10 dB, and draw residual absorption below 3 dB.

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3. Measurements and Results

The experimental setup is illustrated in Fig. 2. The driver and modulator arrays were wire-bond assembled on a custom printed circuit board, providing high-speed signal traces as well as voltage supply and bias connections. The board has cutouts for edge-coupled access using single-mode tapered-lensed fibers positioned with 3-axis precision stages. For all measurements, 1 V and 2 V were provided to V_{DD} and V_{DD2}, respectively. V_{MOD} was independently supplied to each channel, varying from 3.2 to 3.4 V and drawing 3.6 to 4.2 mA of bias current. A pattern generator supplied ac-coupled differential high-speed inputs with ~ 700 mV of peak-to-peak single-ended swing to one channel at a time. The output from a 1310-nm distributed feedback (DFB) laser was passed through a polarization controller and inserted into the corresponding waveguide along the TE polarization. The laser launched 13.6 dBm of continuous-wave power. The output was collected from the chip and sequentially passed through a praseodymium-doped fiber amplifier, a tunable wavelength filter, and a tunable optical attenuator. A sampling scope with a 30-GHz optical plugin module was used to capture the transmitted eye diagrams, while a reference receiver (RX) [7] and bit-error-rate (BER) tester were used to measure BER. Optical amplification is required to overcome coupling losses (~ 7 dB/facet) in both the transmitter and reference RX. A pseudo-random bit sequence of length 2^{31}–1 (PRBS 31) was transmitted during the eye diagram measurements. Due to the low-frequency cutoff of the ac-coupled reference RX which inhibits patterns with long run lengths, a PRBS 15 pattern was transmitted during BER measurements.

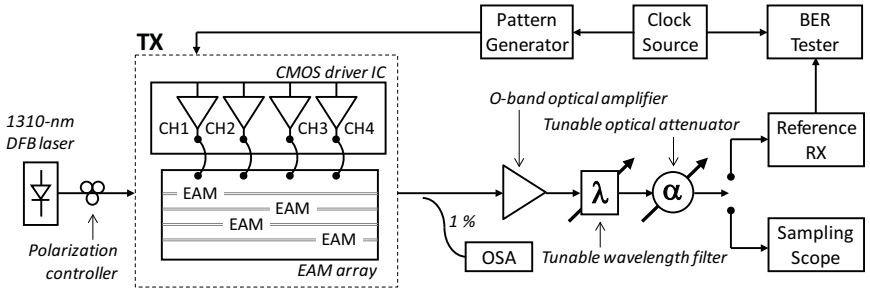

Fig. 2: Block diagram of the experimental setup.

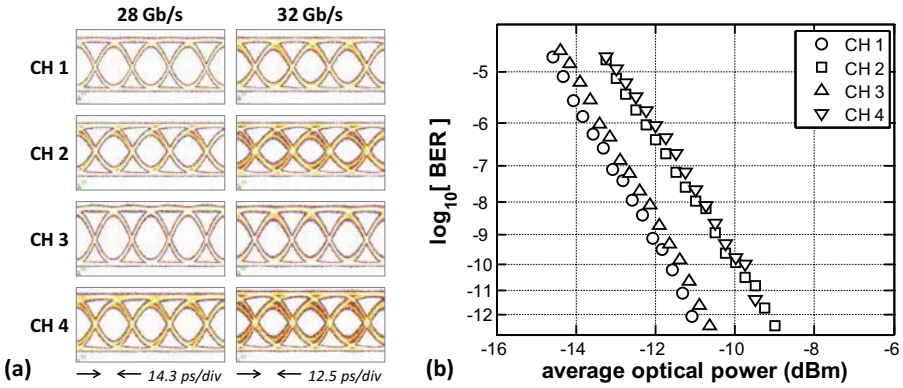

Fig. 3: (a) Measured output eye diagrams for the four transmitter channels at 28 and 32 Gb/s using a PRBS 31 pattern. (b) BER measurements, performed at 32 Gb/s using a PRBS 15 pattern, for all four channels using a reference RX plotted versus received optical power.

The eye diagrams remain open beyond 32 Gb/s for all channels [Fig. 3(a)]. ERs of 9.5 dB, 7.6 dB, 9.4 dB, and 8.2 dB are measured for channels 1 to 4, respectively. Channels 2 and 4 experience a reduction in eye opening compared to channels 1 and 3 due to increased capacitance in the electrical paths connecting to the second and fourth EAMs, which can be alleviated in future designs. The fiber-coupled average optical power of each channel is > -6 dBm under modulation. BER measurements at 32 Gb/s [Fig. 2(b)], demonstrate BER < 10^{-12} for all channels with no indication of an error floor. The inter-symbol interference observed in channels 2 and 4 incurs a penalty of 1.6 dB relative to channels 1 and 3. At 32 Gb/s the total power consumption is 170 mW after subtracting the 20 mW of power resulting from DC currents in the CMOS input terminations. As a point of comparison, state-of-the-art commercially-available four-channel 25/28 Gb/s EAM drivers with 2 V_{pp} output swing consume ≥ 750 mW [8].

4. Wavelength Tunability Demonstration

The previous measurements were performed with a fixed wavelength near 1310 nm for all channels. However, the modulator array is well-suited to operate in both parallel single-mode (PSM) and wavelength-division multiplexed

(WDM) optical links. Fig. 4(a) shows the measured modulator transmission spectra for different applied bias voltages. The absorption edge red-shifts with increasing reverse bias due to the quantum-confined Stark effect, allowing broad wavelength tunability within the O-band. In order to demonstrate the spectral range, we replaced the fixed wavelength DFB laser with a tunable O-band laser, followed by a booster semiconductor optical amplifier and a tunable wavelength filter. Light from the tunable source was passed through channel 1 of the modulator array and modulated at a data rate of 32 Gb/s with a PRBS 31 pattern. The laser and both wavelength filters were tuned in tandem while adjusting V_{MOD} to compensate the wavelength shifts. Figs. 4(b) and 4(c) show optical spectra captured from the optical spectrum analyzer (OSA) and eye diagrams recorded in the same manner as described above at representative wavelengths of 1295 nm and 1320 nm. At 1295 nm 2.1 V is applied to V_{MOD}, and 4 dBm of input power is available from the tunable source. An ER of more than 10 dB is observed, while about 3 dB of insertion loss is added relative to transmission at 1310 nm. At 1320 nm 3.6 V is applied to V_{MOD}, and 8 dBm of input power is available. An ER of 7 dB is observed with fiber-to-fiber loss consistent with the 1310-nm results. The device reported here provides ample spectrum to cover four channels at 5 nm spacing, but could support more channels or larger spacing by integrating III-V materials with varied epitaxial parameters, optimized for different wavelengths.

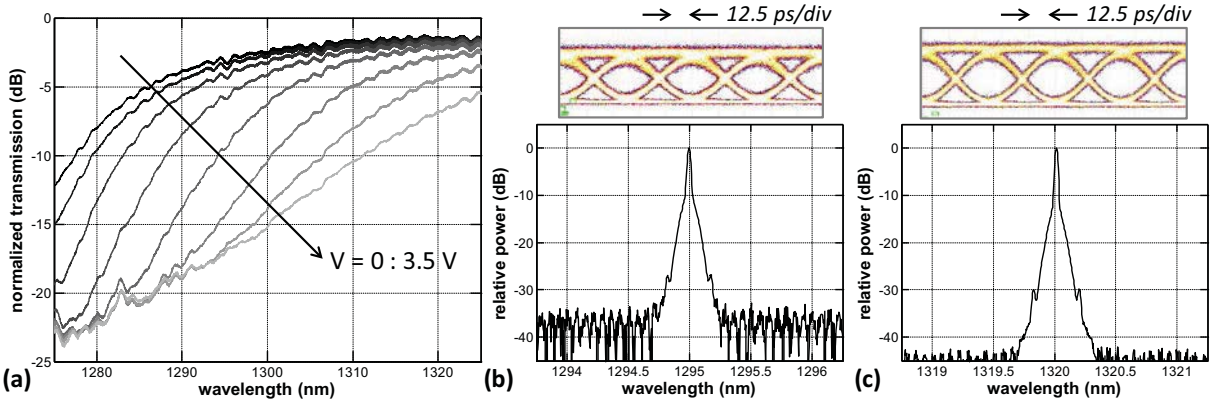

Fig. 4: (a) Transmission spectra at 20° C of the channel-1 EAM for reverse biases from 0 V (black) to 3.5 V (gray) in 0.5 V increments, referenced to a passive silicon waveguide. (b)-(c) Spectra and eye diagrams for a 32-Gb/s signal at a wavelength of 1295 nm (b) and 1320 nm (c).

5. Conclusion

We have demonstrated a four-channel CMOS-driven EAM array operating up to 32 Gb/s per channel with 1.3 pJ/b of electrical power dissipation, representing a significant improvement over the state of the art. Error-free transmission was confirmed for each channel. We further illustrated the suitability of the technology for both PSM and WDM links by investigating performance at various wavelengths.

6. Acknowledgment

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7. References

[1] IEEE P802.3bs 400 Gb/s Ethernet Task Force. (2014). [Online]. Available: http://www.ieee802.org/3/bs/index.html.

[2] T. Pinguet *et al.*, "25 Gb/s silicon photonic transceivers," in *International Conference Group IV Photonics*, (IEEE, 2012), pp. 189-191.

[3] S. Jatar *et al.*, "Performance of parallel 4x25 Gbs transmitter and receiver fabricated on SOI platform," in *International Conference Group IV Photonics*, (IEEE, 2012), pp. 159-161.

[4] B. R. Koch *et al.*, "Integrated silicon photonic laser sources for telecom and datacom," in *Optical Fiber Communication Conference*, (OSA, 2013), paper PDP5C.8.

[5] N. Dupuis *et al.*, "30Gbps optical link utilizing heterogeneously integrated III-V/Si photonics and CMOS circuits," in *Optical Fiber Communication Conference*, (OSA, 2014), paper Th5A.6.

[6] T. Woodward *et al.*, "Modulator-driver circuits for optoelectronic VLSI," *IEEE Photon. Technol. Lett.* **9**, 839-841 (1997).

[7] B. G. Lee *et al.*, "60-Gb/s receiver employing heterogeneously integrated silicon waveguide coupled photodetector," in *Conference Lasers Electro-Optics*, (OSA, 2013), paper CTh5D.4.

[8] MACOM Product Detail: MAOM-02204A. (2014). [Online]. Available: http://www.macom.com/products/product-detail/MAOM-02204A.