Energy-Aware Signal Integrity Analysis for High-Speed PCB Links

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***Abstract*—This paper proposes a novel approach to evaluate design alternatives for high-speed links on printed circuit boards. The approach combines evaluations of signal integrity and link input power. For a comprehensive analysis, different link designs are made comparable through the application of identical constraints, with the link input power as the single figure of merit for a systematic, quantitative comparison of design alternatives. The analysis relies upon a combination of efficient physics-based via and trace models, statistical time-domain simulation, and an analytical input power evaluation, which allows it to handle links consisting of a large number of channels while fully taking into account interchannel crosstalk. The proposed approach is applied to study two fundamental design decisions at the PCB level—single-ended versus differential signaling and signal-to-ground via ratios of 1:1 versus 2:1—for a link consisting of 2048 vias and up to 175 striplines with an aggregate data rate of 1 Tb/s. It is found that both design decisions have a considerable impact on the required input power of the link.**

***Index Terms*—Energy-aware analysis, high-speed links, printed circuit boards (PCBs), signal integrity (SI), via arrays.**

I. Introduction

With data rates currently targeting 25–28 Gb/s per channel for midrange electrical interconnects [1], guaranteeing signal integrity (SI) for proper functioning of electrical links on printed circuit boards (PCBs), as shown in Fig. 1, remains a challenge [2]. Increasing high-frequency spectral content of signals increases both transmission loss and interchannel crosstalk, posing severe challenges to maintaining SI. This development necessitates a continuous optimization of interconnect designs. Since design changes of PCB interconnects typically involve a complex tradeoff between several competing requirements, such a design optimization requires tools and methods that facilitate a fast and systematic SI analysis and comparison of design alternatives. Tools that can contribute to the fast analysis are physics-based via and trace models, as studied in [3]–[5].

Exacerbating the described challenges with regard to SI, the rising power consumption of digital systems [6] steadily increases the need for energy-aware design of I/O links, which currently account for about 20% of CPU power dissipation—with a predicted increase to 50% in 2020 [7]. Over the past decade, several approaches have been presented that aim at energy efficiency optimization of electrical links. They can be divided into those focusing on on-chip links, e.g., [8]–[12] and those focusing on off-chip links, e.g., [13]–[19]. For on-chip links, comparatively simple interconnect models such as distributed *RC* models [9] can be employed. For off-chip links, in contrast, the complex characteristics of PCB interconnects require much more elaborate models. This problem is often circumvented by using measured interconnect data [13]–[15]. While measured data provides a realistic interconnect model, it limits the study to an optimization of transmitter and receiver circuits for a specific interconnect design, and broad insights are often difficult to obtain. Other studies use generic interconnect models [16]–[19] to obtain general insights, but to the knowledge of the authors, no approach has yet focused on improving the energy efficiency of specific off-chip interconnect designs.

In this paper, a method is proposed that combines a systematic SI analysis with an evaluation of energy efficiency to find improved off-chip interconnect design solutions. The method is built upon efficient modeling and analysis approaches, which

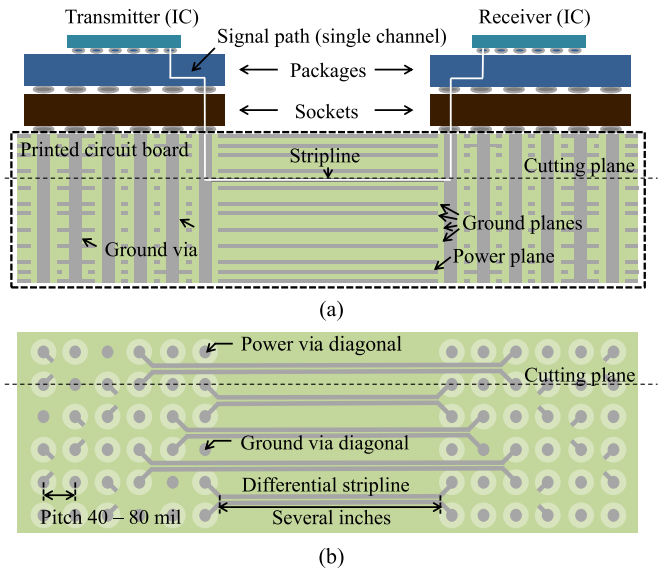

Fig. 1. Schematic of a PCB link (drawings are not to scale). (a) Side view of the overall interconnect system consisting of the integrated circuits (ICs), packages, sockets, and PCB. (b) Top view of a PCB cross section through a signal layer (outer vias routed on a lower layer). Typical designs include several hundreds to thousands of vias and stripline lengths of several inches.

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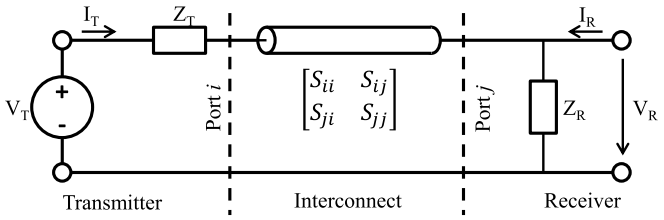

Fig. 2. Channel model employed for the input power evaluation. The interconnect is modeled by its *S*-parameters, from which the *ABCD* parameters can be obtained. Transmitter and receiver are taken into account through their termination impedances.

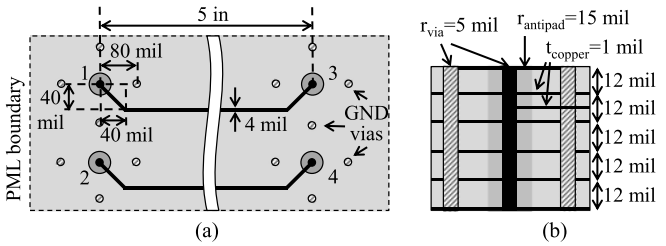

Fig. 3. (a) Top view and (b) cross section of a simple test link to demonstrate the impact of ground vias on SI and link input power. Material parameters are $\sigma = 5.8 \times 10^7$ S/m for copper and $\varepsilon_r = 3.6$ and $\tan(\delta) = 0.02$ for the dielectric substrate. Simulations are carried out with a PML boundary condition.

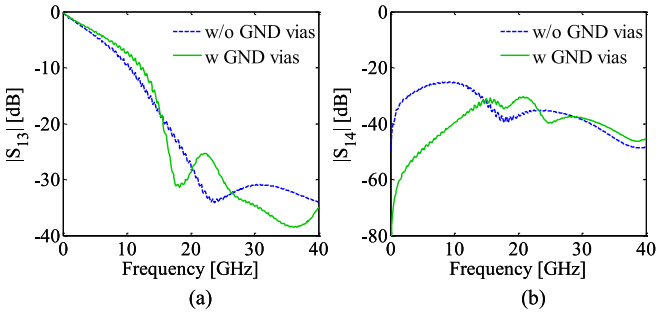

Fig. 4. *S*-parameters of the PCB link in Fig. 3, simulated without and with ground vias, showing (a) transmission and (b) far-end crosstalk. The ground vias clearly improve SI for frequencies up to 15 GHz.

allow studying complex off-chip links with moderate effort. A quantitative comparison between design alternatives is facilitated by using a single figure of merit similar to [20]; however, the link input power is chosen here as the figure of merit, leading to an energy-aware SI analysis. The remainder of this paper is organized as follows: Section II uses a simple example to illustrate an energy-aware evaluation. Section III describes an approach for a systematic, energy-aware SI analysis and the methods that are used to carry out the different steps in an efficient way. Section IV demonstrates the evaluation of design alternatives for a 1 Tb/s link. Section V summarizes the conclusions with regard to applicability of the proposed approach and to findings for the studied link example.

II. Energy-Aware Evaluation

In this section, an analytical link input power evaluation based on an equivalent circuit is described. It is then applied to a simple test case in order to motivate the energy-aware SI analysis described in Section III.

A. Equivalent Circuit for Power Evaluation

For an analytical input power evaluation, this paper will model each channel of a link by the simplified equivalent circuit in Fig. 2. The interconnect channel is represented by the corresponding entries of the *S*-parameter matrix. Transmitter and receiver are modeled by impedances Z_T and Z_R, which represent the corresponding output and input impedances, including any terminations. The applied equivalent circuit neglects any power overhead in the transmitter and receiver circuits, aiming at a general evaluation of the relation between interconnect properties and input power rather than evaluations of specific circuit designs. The simplicity of the model permits a convenient evaluation in terms of ABCD parameters, which relate voltages and currents at transmitter and receiver as [21]

$$\begin{pmatrix} V_R \\ I_R \end{pmatrix} = \begin{bmatrix} 1 & 0 \\ 1/Z_R & 1 \end{bmatrix} \cdot \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} 1 & Z_T \\ 0 & 1 \end{bmatrix} \cdot \begin{pmatrix} V_T \\ -I_T \end{pmatrix} \tag{1}$$

with the *ABCD* parameters of the interconnect obtained from the corresponding *S*-parameters and other quantities as specified in Fig. 2. With $I_R = 0$ (since the receiver input impedance is included in the value of Z_R), the input impedance of the complete channel model becomes [21]

$$Z_{\text{in}} = \left(\frac{V_T}{I_T}\right) = Z_T + \frac{B/Z_R + D}{A/Z_R + C}. \tag{2}$$

For a given transmitter output voltage V_T, (2) allows one to calculate the channel input power as well as the current I_T. Subsequently, (1) can be solved for the voltage V_R seen at the receiver. The knowledge of all voltages and currents then allows evaluation of the power dissipation separately for Z_T, Z_R, and the interconnect itself. It should be noted that due to the frequency dependent interconnect network parameters, the input impedance and the dissipated power are also frequency dependent—even in case of constant Z_T and Z_R.

B. Evaluation for a Simple Test Case

In this section, an energy-aware evaluation is carried out for a simple test case. The impact of a change in the interconnect design is studied as well as the impact of the termination impedances. The detailed setup of the test case is shown in Fig. 3. The test link consists of two single-ended channels, each formed by a stripline connecting two signal vias over a distance of 5 in. To study the impact of an interconnect design change, the link is simulated without and with the ground vias shown in Fig. 3. The impact of the ground vias on SI can be seen in the *S*-parameters of the interconnect. The *S*-parameters have been obtained from physics-based via and trace models [22], as described in detail in Section III-B, and are normalized to 50 Ω. Up to about 15 GHz, the ground vias improve the transmission in Fig. 4(a) and clearly reduce the far-end crosstalk in Fig. 4 (b) by providing a conductive return path for the signal currents.

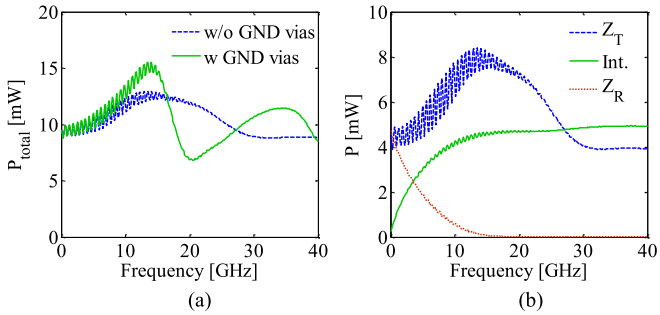

Fig. 5. Evaluation of input power for one channel of the PCB link in Fig. 3, using the calculation approach described in [21]. (a) Comparison of the total link input power $P_{\mathrm{total}} = V_T^2 \cdot \mathrm{Re}\{Z_{\mathrm{in}}^{-1}\}$, for $V_T = 1$ V for the configurations without and with ground vias. Below 16 GHz, the ground vias lead to an increase in link input power. (b) Frequency-dependent power dissipation in the different elements in the scenario without ground vias.

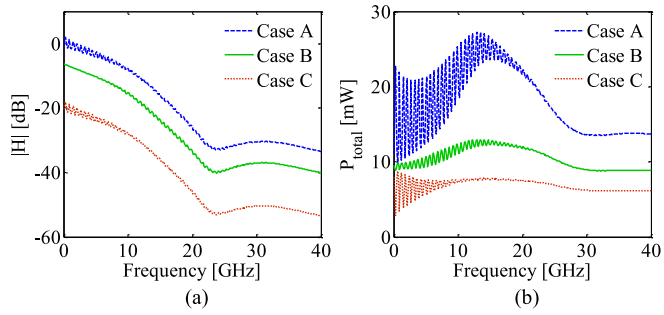

Fig. 6. Evaluation of one channel of the PCB link in Fig. 3 (interconnect characteristic impedance close to 50 Ω) for different termination scenarios. A: $Z_T = 10\ \Omega$, $Z_R = 100\ \Omega$; B: $Z_T = 50\ \Omega$, $Z_R = 50\ \Omega$; C: $Z_T = 100\ \Omega$, $Z_R = 10\ \Omega$. (a) Voltage transfer function $H = V_R/V_T$ and (b) total link input power for $V_T = 1$ V. Case A results in the highest voltage transfer function, case C in the lowest link input power.

At higher frequencies, the ground vias introduce additional resonances, since they resemble a resonant cavity around each signal via. While the impact on SI in this higher frequency range is not obvious from the *S*-parameters, ground vias clearly improve the integrity of signals with spectra mainly below 15 GHz.

For an energy-aware evaluation, the *S*-parameters of the interconnect are now supplemented by the input power calculated for the equivalent circuit in Fig. 2. For one channel of the test link, Fig. 5(a) compares the total input power for the configurations without and with ground vias ($V_T = 1$ V, $Z_T = Z_R = 50\ \Omega$). The plot illustrates that the overall dissipated power is not only frequency dependent but also strongly influenced by the interconnect configuration, which changes the input impedance of the equivalent circuit. The input power can be broken down further to the power dissipated by the individual elements of the equivalent circuit, as shown in Fig. 5(b). At very low frequencies, the dissipated power is shared evenly between Z_T and Z_R. With increasing frequency, an increasing part of the power is dissipated in the interconnect, while a decreasing part reaches the receiver. Of the additional input power due to a lower input impedance around 13 GHz, only a small part reaches the interconnect while the largest part is dissipated in the transmitter impedance.

Obviously, not only the interconnect design but also Z_T and Z_R can be varied. Instead of renormalizing the *S*-parameters, Fig. 6(a) directly shows the voltage transfer function between transmitter and receiver for different scenarios where the termination impedances are modified while the interconnect characteristic impedance remains unchanged (close to 50 Ω). While the highest transfer function is obtained for a high receiver impedance, the lowest input power is obtained for a high transmitter impedance, as illustrated by Fig. 6(b). In general, a variation of Z_T and Z_R as well as the characteristic impedance of the interconnect will provide a large design space for tradeoffs between SI and energy efficiency. The remainder of this paper focuses on an analysis of interconnect design variations in a 50 Ω system, which allows a more intuitive analysis in terms of *S*-parameters. Even with this restriction, the analysis remains complex, as illustrated by the findings for the studied test link. From a SI perspective, the ground vias lead to a clear improvement at least for signals with spectra below 15 GHz. However, leaving all other things equal, they also lead to an increased input power, most of which is dissipated in Z_T and does not reach the interconnect. For via arrays as used in high speed links (see Fig. 1), ground vias come with additional tradeoffs, since they take up space in the grid. For a constant packaging area, this means that the number of channels for signal transmission is reduced, and the data rate at which the individual channels are operated has to be increased to keep the aggregate data rate constant—typically with a negative impact on SI. On the other hand, a lower number of channels will reduce the total link input power. Other design variations may be even more difficult to analyze, with a frequency dependent impact on transmission, crosstalk, and input power that may differ from channel to channel. This complexity creates the need for a systematic SI analysis that takes into account the impact of design changes on energy efficiency.

III. Approach for a Comprehensive Analysis

In this section, an approach for a systematic, energy-aware SI analysis for PCB links is presented. The general concept of the method is described first, followed by more detailed descriptions of the individual building blocks.

A. General Description of the Proposed Approach

For a meaningful comparison of different designs, the proposed approach defines objective functions based on the tradeoffs discussed in Section II. For instance, the main objective function is the bit error rate, which is the ultimate parameter to determine the SI properties of the link. To compare different designs, the aggregate data rate of the link and the packaging area occupied by the link are introduced as additional objective functions. It is assumed that target values for all three quantities are given prior to the analysis (e.g., fixed in an early stage of the design process). This leaves the link input power, which is used to measure the energy efficiency of the link, as the single figure of merit for the comparison of different design alternatives. In other words, the optimal link design is the one which meets the specified objectives in the most energy efficient way. To evaluate the link input power required by a certain design alternative, the proposed method follows three steps, as depicted in Fig. 7. First, a network parameter description of the complete

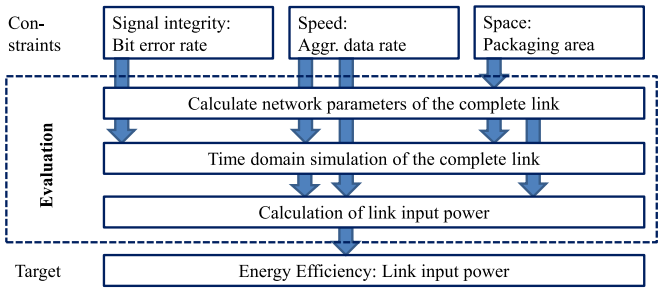

Fig. 7. Proposed approach for a systematic, energy-aware SI analysis of PCB links. The evaluation consists of a network parameter calculation, a time-domain evaluation, and a link input power calculation. The optimal design fulfills the constraints with the lowest input power.

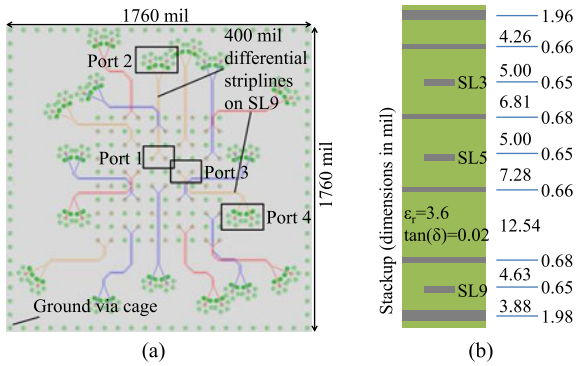

Fig. 8. PCB test structure for modeling with physics-based via and trace models: via array with connected striplines. (a) Top view and (b) stackup. SL3, SL5 and SL9 are the signal layers on which striplines are routed.

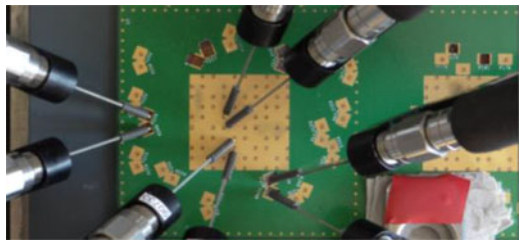

Fig. 9. PCB test structure with microprobe setup for 8-port measurement using a 12-port vector network analyzer (10 MHz–50 GHz). The microprobes (GS- and SG, 225 μm pitch) have been calibrated up to the probe tips on CS-14 calibration substrate obtained from the probe vendor.

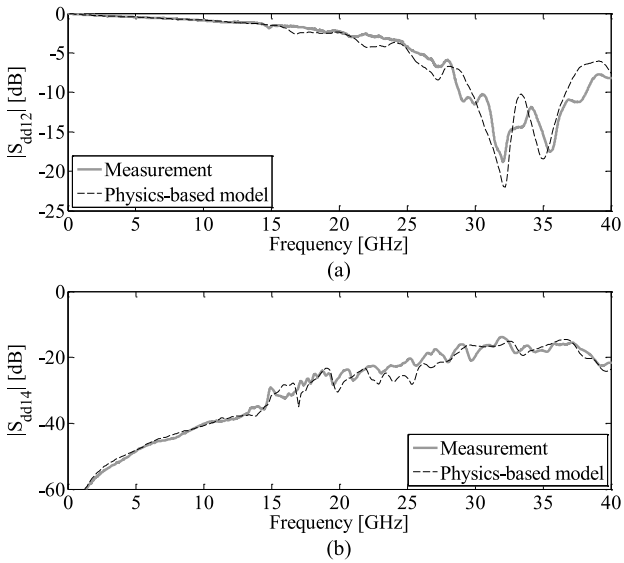

Fig. 10. Comparison between *S*-parameters from measurement and physics-based models for (a) differential transmission between port 2 and port 1 and (b) differential far-end crosstalk (FEXT) between port 4 and port 1 [location of differential ports shown in Fig. 8(a)].

link is obtained, including the interaction between all channels. In a second step, a time-domain analysis is carried out to determine the minimum transmitter output voltage swing for which all channels in the link meet the required bit error rate. Based on the determined voltage swing, the required link input power for the specific design alternative is calculated in a third step. Since a meaningful evaluation has to take into account all channels in the link—including inter channel crosstalk—highly efficient methods are required for each step of the proposed method in order to study links of a realistic size. In the following sections, suitable methods are described together with the assumptions made in this paper.

B. Calculation of Interconnect Network Parameters

An efficient yet sufficiently accurate method to calculate a complete network parameter description of PCB interconnects is the application of physics-based via and trace models. Since these models are largely based on analytical formulas, they are considerably faster (between two and three orders of magnitude) and more memory efficient than general purpose numerical methods. In this paper, the algorithm described in [22] is used with the parallel plate admittance calculated from the contour integral method (CIM) with radial ports and infinite planes [23], [24], and the via near-field model calculated according to Williamson [25]. Trace models are calculated with a fast two-dimensional (2-D) numerical method [26] and included as described in [3] based on a modal decomposition approach [27].

The accuracy of physics-based models has been extensively studied in several papers, e.g., [3] and [28]. For via-arrays with 80 mil pitch, which will be employed in all examples in this paper, good agreement with measurement and full-wave results has been observed for frequencies up to 40 GHz [28]. Here, additional model validation is carried out for the differential test site depicted in Fig. 8. Differential striplines of 400 mil length are connected to vias inside a 10 $\times$ 10 via array and launch vias outside the array. The microprobe setup for an eight-port measurement (four differential ports) is shown in Fig. 9. Both the differential transmission along a channel in Fig. 10(a) and the differential far-end interchannel crosstalk in Fig. 10(b) show reasonable agreement between measurement and simulation in the frequency range up to 40 GHz. Based on our experience, in this frequency range, the effect of inaccuracies in the physics-based models is not larger than the uncertainty caused by production tolerances and variations in material properties, which makes the physics-based models a suitable choice for a fast network parameter calculation. A DC point, which cannot be calculated using the physics-based models, can be obtained from a linear extrapolation of both magnitude and phase of the calcu-

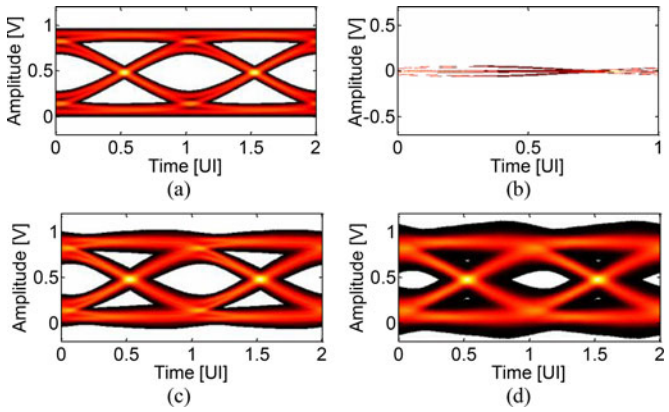

Fig. 11. Eye diagrams at 15 Gb/s for different cases ($V_{\max} = 1$ V). (a) Statistical eye diagram for a single channel without impact of crosstalk. (b) "Crosstalk eye diagram" for far-end crosstalk from a neighboring channel. (c) Eye diagram with far-end crosstalk from one neighboring channel. (d) Eye diagram with far-end crosstalk from five neighboring channels.

lated *S*-parameters, or from an analytical approximation based on the trace resistance. Both approximations lead to very similar results for the evaluation in Section IV-B.

C. Statistical Time-Domain Simulation Including Crosstalk

A suitable calculation method for an efficient time-domain simulation is the statistical approach presented in [29] and [30]. In this approach, the eye diagram is a 2-D probability density map showing the likelihood of a certain receiver voltage level at a certain point in time. The basic eye diagram of a channel is constructed from its pulse response, which can be calculated from its *S*-parameters. A discretization of time and voltage in the practical implementation leads to a binning of voltage levels at each time step. The advantage of the statistical approach is the efficient inclusion of crosstalk with known and unknown phase offset. To account for the impact of crosstalk on a channel, a "crosstalk eye diagram" is constructed from the corresponding entry of the *S*-parameter matrix and convolved with the channel eye diagram. The convolution of two discretized eye diagrams is described by

$$f(\tau, v) = f_1(\tau, v) * f_2(\tau, v) = \sum_{v'=1}^{N} f_1(\tau, v') \cdot f_2(\tau, v - v') \tag{3}$$

with horizontal pixel index τ (discretized time), vertical pixel index v (discretized voltage), number of vertical pixels N, and pixel probability $f(\tau,v)$ (probability that the voltage is in bin v at time step τ). Aggressors with an unknown phase shift can be included through a time-independent histogram of voltage levels [30]. An example for the addition of crosstalk to an eye diagram is shown in Fig. 11. Different colors indicate different probabilities; white areas have probabilities below the target bit error rate, which is 10^{-12} for this paper. All time-domain evaluations in this paper assume a random non-return-to-zero (NRZ) signal with lower voltage level $V_{\min} = 0$ V, tunable upper voltage level $V_{\max}$, and probabilities of $p = 0.5$ for both levels. At the transmitter output, bits have a trapezoidal shape with rise and fall time each corresponding to 10% of the unit interval (UI). The goal of the time-domain analysis is to find the minimum transmitter output voltage swing for which all channels meet the required bit error rate. The search is carried out in two steps. First, the eye diagrams for all channels are calculated. For the worst-case channel (smallest vertical eye opening), the required input voltage swing is calculated from the actual eye opening and the target value, and the simulation of the worst-case channel is repeated. All simulations fully take into account interchannel crosstalk. Similar to [16]–[19], a continuously variable transmitter voltage swing is assumed to find the theoretical optimum for the link input power. The required input voltage swing has been found as soon as the target eye opening is met. Due to the linearity of the system, only one or two iterations are necessary.

All evaluations in this paper are carried out without equalization. Further investigations may include one or more equalization schemes to study their impact on the link input power for different link designs. In principle, the proposed method can also be used to study the impact of alternative signal encodings (e.g., PAM 4) on the energy efficiency of signal transmission, including the complete impact of crosstalk from all channels in the link.

D. Analytical Input Power Evaluation

In Section II-B, the frequency-dependent link input power was calculated using the channel model in Fig. 2. The channel input power for a given NRZ signal as defined in Section III-C can be obtained from integration of the power spectral density P_{xx} (V^2/Hz) of the signal over frequency, taking into account the input impedance of the channel as described later. For the random NRZ signals assumed here (see Section III-C: voltage levels 0 and $V_{\max}$ and probability $p = 0.5$ for each level), the power spectral density is given in [31] as

$$P_{XX}(f) = \frac{\left|\tilde{F}(f)\right|^2}{4T_b} \cdot \left(1 + \frac{2\pi}{T_b} \sum_{n=-\infty}^{\infty} \delta\left(2\pi f - \frac{2\pi n}{T_b}\right)\right) \tag{4}$$

with the bit period T_b and the Fourier transform of a single bit $\tilde{F}(f)$. For a trapezoidal shape with 10% rise and fall time, the Fourier transform of a single bit is [32]

$$\tilde{F}(f) = V_{\max} \cdot T_b \cdot \operatorname{sinc}(fT_b) \cdot \operatorname{sinc}\left(\frac{fT_b}{10}\right). \tag{5}$$

Subsequently, the one-sided power spectral density P_{XX}^{SS} is used, with $P_{XX}^{SS}(0) = P_{XX}(0)$ and $P_{XX}^{SS}(f) = 2P_{XX}(f)$ if $f > 0$. The input power P of a channel with input impedance Z_{in} for the assumed input signal can be obtained from

$$P = \int_0^{\infty} P_{XX}^{SS}(f) \cdot \operatorname{Re}\{Z_{\text{in}}^{-1}(f)\} df \tag{6}$$

by inserting (2), (4), and (5). From (4), it can be seen that the power spectral density consists of a continuous and a discrete part. For the chosen input signal, the discrete part only exists at $f = 0$ Hz due to zeroes in the single-bit Fourier transform at higher frequencies. The contribution of the continuous part to the input power in (6) is evaluated through numerical integration for the analysis in this paper: S, Z_{in}, and the continuous part of

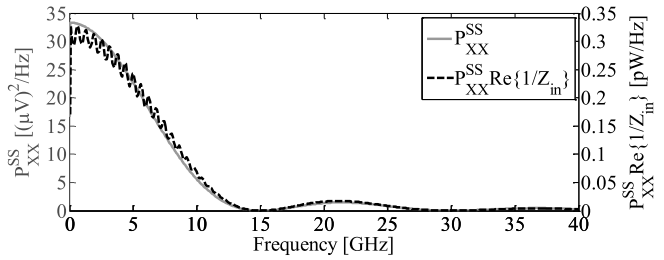

Fig. 12. Input power evaluation for one channel of the test link in Fig. 3, for a data rate of 15 Gb/s and $V_{\max} = 1$ V. The plot shows the one-sided power spectral density of the signal before and after division by the real part of Z_{in}. Numerical integration up to 40 GHz gives an input power of 2.43 mW, of which the frequencies up to 15 GHz contribute 2.27 mW.

P_{XX}^{SS} are calculated for equally spaced frequency points from 0 to 40 GHz with $\Delta f = 100$ MHz, and the integral is replaced with a sum and *df* with Δf in (5). The total link input power is obtained by summation of discrete and continuous contributions for all channels. An example for the input power evaluation is given in Fig. 12.

It shall be pointed out that the calculated power contains only the power dissipated in the interconnect itself and in the termination impedances (Z_T and Z_R), which include the output impedance of the transmitter and the input impedance of the receiver. Any overhead due to losses inside the transmitter and receiver circuits is not taken into account. Furthermore, the power calculation for differential cases assumes a purely differential signal without any offset voltage. These simplifications allow for a comparatively simple evaluation. They make it possible to observe general trends independently of specific transmitter and receiver designs, and provide the fundamental limits that will be approached as circuit overhead is shrunk to reduce power. Future work will address the inclusion of more realistic models for transmitter and receiver circuits. While such models can be included in the general approach depicted in Fig. 7 by using numerical circuit simulators for the time-domain and power evaluation, the challenge is to find simulation approaches that sustain the high efficiency provided by the analytical evaluation for the simplified model.

IV. Application to a Test Case

To demonstrate the capabilities of the employed methods, the approach outlined in Section III is applied in this section to evaluate design alternatives for a 1 Tb/s PCB link consisting of a large number of vias and channels.

A. Setup

The basic test structure setup is shown in Fig. 13: Two via arrays—each consisting of 32 × 32 vias with 80 mil pitch—are placed 5 in apart from each other. Signal vias inside the triangular sections highlighted in Fig. 13 are connected by striplines to form a 1 Tb/s link. Signal vias outside the highlighted sections are assumed to belong to other links and are terminated with 50 Ω for the simulation. To reduce simulation times and make the results independent of specific PCB dimensions, a perfectly matched layer (PML) boundary condition is used for all simulations. Four design alternatives are evaluated based on two fundamental design decisions: the signaling scheme (single-ended versus differential) and the signal-to-ground ratio (1:1 versus 2:1). In the following, the four designs will be referred to as SE11, SE21, Diff11, and Diff21. For all designs, the upper edge of the triangular section in Fig. 13 is formed by ground vias, and the right array is a mirrored version of the left one. Furthermore, the three to four via rows closest to the edges of the array are routed on the first signal layer, the next rows on the second signal layer, and so on. All vias are assumed to span the entire PCB stackup and are not backdrilled. The detailed arrangements of vias and striplines depend on the specific design and are illustrated in Fig. 14. All designs use the stackup shown in Fig. 15.

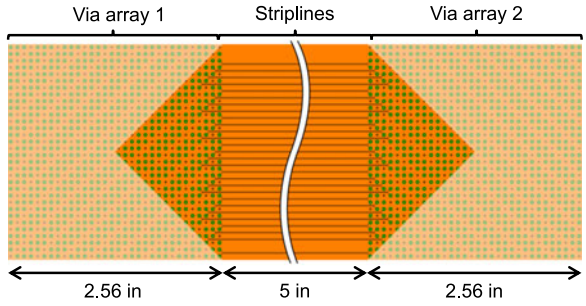

Fig. 13. Illustration of the basic link setup for the case Diff11 (see Fig. 14 for detail) with all vias. The vias inside the highlighted triangular region form the 1 Tb/s link.

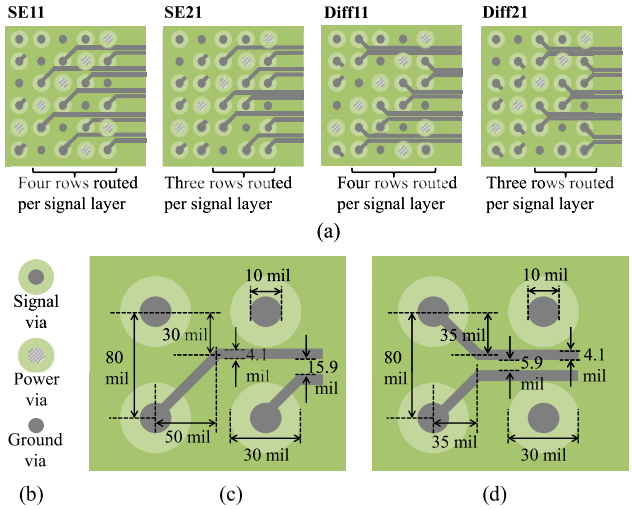

Fig. 14. (a) Arrangement of signal, power, and ground vias for the different scenarios; (b) via types; and detailed via and trace geometries for (c) single-ended and (d) differential transmission.

As a basis for the evaluation, the *S*-parameters of the structure were calculated using physics-based via and trace models as described in Section III-B. Simulation times with the parallel code (processor: AMD Opteron 6140, 2.6 GHz) are listed in Table I. It should be noted that evaluation times for smaller test cases will be much lower. Results for the transmission and far-end crosstalk of a channel inside the array are shown in Fig. 16. The transmission shows resonances due to the via stubs and the ground via pattern. The far-end crosstalk shows clear differences between the designs up to about 15 GHz, but a more complex

Layer number	Thickness [mil]	Assignment	Layer number	Thickness [mil]	Assignment	Layer number	Thickness [mil]	Assignment
1	**2.1**	Ground	13	**0.7**	Ground	25	**0.7**	Signal 5
2	**7.5**	Substrate	14	**4.4**	Substrate	26	**4.4**	Substrate
3	**0.7**	Power	15	**0.7**	Signal 3	27	**0.7**	Ground
4	**3.7**	Substrate	16	**3.8**	Substrate	28	**3.8**	Substrate
5	**0.7**	Ground	17	**0.7**	Ground	29	**0.7**	Signal 6
6	**4.4**	Substrate	18	**7.5**	Substrate	30	**4.4**	Substrate
7	**0.7**	Signal 1	19	**0.7**	Ground	31	**0.7**	Ground
8	**3.8**	Substrate	20	**3.8**	Substrate	32	**3.7**	Substrate
9	**0.7**	Ground	21	**0.7**	Signal 4	33	**0.7**	Power
10	**4.4**	Substrate	22	**4.4**	Substrate	34	**7.5**	Substrate
11	**0.7**	Signal 2	23	**0.7**	Ground	35	**2.1**	Ground
12	**3.8**	Substrate	24	**3.8**	Substrate			

Fig. 15. Stackup used for all simulated cases (right columns continue the left column). If less than six signal layers are needed, lower signal layers remain unused. Material parameters are $\sigma = 5.8 \times 10^7$ S/m for copper and $\varepsilon_r = 3.6$ and $\tan(\delta) = 0.02$ for the dielectric substrate.

TABLE I
COMPARISON OF SIMULATION TIMES

	SE11	SE21	Diff11	Diff 21
S-parameters—16 cores [h]	19.7	20.5	19.2	19.7
Time domain—8 cores [h]	16.0	20.0	7.5	10.4

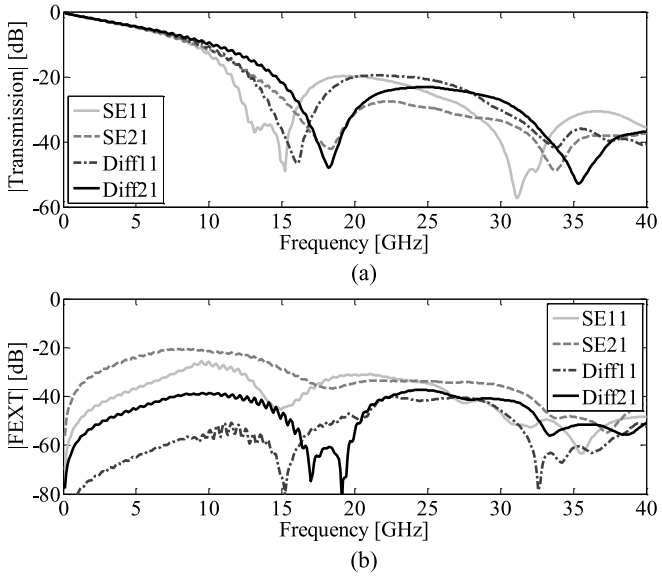

Fig. 16. (a) Transmission and (b) far-end crosstalk from a neighboring channel for a channel inside the array. Up to about 15 GHz, differential signaling leads to substantially smaller crosstalk than single-ended signaling, and a higher signal-to-ground ratio increases the crosstalk level. Above 15 GHz, however, the crosstalk behavior becomes more complex.

frequency dependent behavior at higher frequencies. Channels at other positions show a different behavior—especially those routed on different signal layers and close to the edges of the array, which see different local environments. This underlines the difficulty of quantitatively comparing different designs using *S*-parameter curves only.

B. Results of Input Power Evaluation

Based on the *S*-parameters, time-domain simulations are carried out as the second step of the evaluation proposed in Section III. The goal is to find the minimum input voltage swing

TABLE II
EVALUATION OF THE DESIGN ALTERNATIVES IN FIG. 14

	SE11	SE21	Diff11	Diff21	Diff21 backdr.
Number of channels	135	175	64	85	85
Channel data rate (Gb/s)	7.41	5.71	15.63	11.76	11.76
Req. voltage swing (mV)	187	181	276	227	230
Total link power (mW)	**23.4**	**28.3**	**12.4**	**10.9**	**10.8**
Req. voltage swing (mV) -ext. noise $\sigma = 100$ mV	279	260	337	299	302
Total link power (mW) -ext. noise $\sigma = 100$ mV	**52.3**	**58.3**	**18.5**	**19.0**	**18.6**

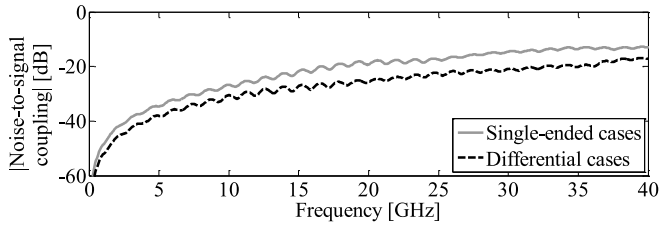

Fig. 17. Transfer functions assumed for noise coupling into signal ports for the single-ended and differential cases based on simulations in [32].

required to meet a specific vertical eye opening at the link output. Here, the target vertical eye opening is set to 100 mV for a bit error rate of 10^{-12}. The target aggregate data rate is 1 Tb/s for all design alternatives. The resulting single-channel data rates for the different designs are listed in Table II. All simulations fully include crosstalk between all channels in a link. Moreover, they are carried out without and with an external noise model (Gaussian noise with 100 mV standard deviation) to study the impact of additional noise sources that will exist in a real system (e.g., power supply noise or crosstalk from other components). For addition of the external noise to the channels, the transfer functions in Fig. 17 are assumed based on coupling between power and signal ports observed in [33]. Simulation times of the time-domain simulation (including noise) with a parallel code (processor: AMD Opteron 6140, 2.6 GHz) are listed in Table I. The required input voltage swings found in the time-domain evaluation are given in Table II. Differences between design alternatives are a result of different transmission and crosstalk properties of the links and of the different data rates at which they are operated. To illustrate the outcome of the time-domain evaluation, eye diagrams for the four design alternatives are shown in Fig. 18 for the respective final voltage swing. As the final step of the proposed evaluation, the input voltage swings found in the time-domain analysis are inserted into the link input power evaluation described in Section III-D. The results in Table II show that in spite of the higher input voltage swing, the input power for differential signaling is only about 50% of that for single-ended signaling. In the power evaluation, the differential designs benefit from the lower number of channels and from the assumption of a purely differential signal. For the signal-to-ground ratio, the difference is smaller, but may be even more relevant, since comparisons can be made among cases with identical signaling. Changing only the signal-to-ground ratio in

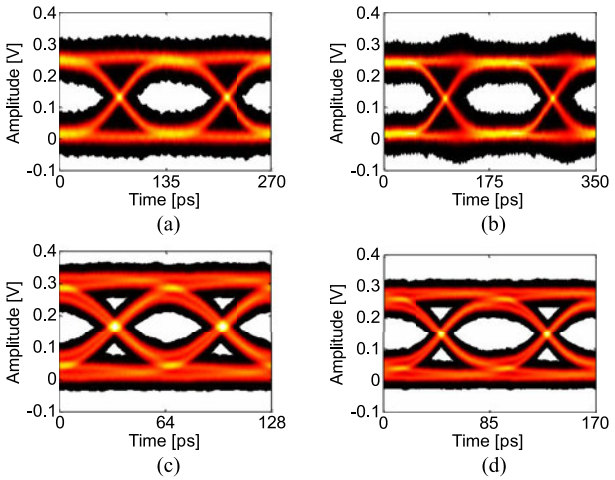

Fig. 18. Statistical eye diagrams including crosstalk and noise for the worst-case channels of the different designs: (a) SE 11, (b) SE 21, (c) Diff 11, and (d) Diff 21. Although crosstalk and external noise have a smaller impact on the differential designs, the differential cases need higher input voltage swings due to the higher data rates at which they have to be operated (see Table II).

otherwise equal designs changes the required link input power by up to 17%. The optimal signal-to-ground ratio depends on the chosen signaling scheme and the noise environment, showing that finding the optimal ratio is not trivial.

In addition to the comparison of fundamental design alternatives, the proposed approach can be applied to evaluate the impact of changes to a given design. As an example, the case Diff 21 is changed by backdrilling of all signal vias (up to the reference plane below the connected trace). Backdrilling removes the via stub resonances visible in Fig. 16(a) from the transmission—in exchange for a higher manufacturing cost. For the case Diff21, however, the required input voltage swing listed in Table II hardly changes for the backdrilled case. The reason is that the worst-case channel at the center of the via array is routed on the lowest signal layer anyway, and therefore is hardly affected by removing the via stub. The critical factor that has to be tackled for the worst-case channel is crosstalk from surrounding channels, not the via stub resonances. Although backdrilling somewhat reduces the required input power due to changes in the input impedances of channels routed at higher layers, its benefit is much smaller than expected in the studied case.

V. Conclusion

As a main contribution, the energy-aware SI analysis presented in this paper makes different link designs quantitatively comparable with a single figure of merit. While the approach still contains several simplifications, it represents a major step toward a systematic comparison and optimization of different link design alternatives including detailed passive interconnect models. It should be mentioned that the best design alternative is not always the one with the lowest input power. Rather, the method allows the designer to trade off a reduction in link input power against additional implementation effort or higher production cost. In this way, it becomes possible to decide if an additional investment e.g., into a higher layer count, a low loss substrate or the backdrilling of vias makes sense. Further work may address a more realistic modeling of receiver and transmitter, which will allow studying the impact of modeling assumptions, e.g., on the differences in required input power observed between the single-ended and the differential cases.

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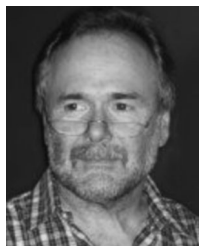

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