30-Gb/s Optical Link Combining Heterogeneously Integrated III–V/Si Photonics With 32-nm CMOS Circuits

Nicolas Dupuis, Benjamin G. Lee, *Senior Member, IEEE*, Jonathan E. Proesel, *Member, IEEE*, Alexander Rylyakov, Renato Rimolo-Donadio, *Member, IEEE*, Christian W. Baks, Abhijeet Ardey, Clint L. Schow, *Senior Member, IEEE, Senior Member, OSA*, Anand Ramaswamy, Jonathan E. Roth, Robert S. Guzzon, Brian Koch, Daniel K. Sparacin, *Member, IEEE*, and Greg A. Fish, *Senior Member, IEEE*

***Abstract*—We present a silicon photonics optical link utilizing heterogeneously integrated photonic devices driven by low-power advanced 32-nm CMOS integrated circuits. The photonic components include a quantum-confined Stark effect electroabsorption modulator and an edge-coupled waveguide photodetector, both made of III–V material wafer bonded on silicon-on-insulator wafers. The photonic devices are wire bonded to the CMOS chips and mounted on a custom PCB card for testing. We demonstrate an error-free operation at data rates up to 30 Gb/s and transmission over 10 km at 25 Gb/s with no measured sensitivity penalty and a timing margin penalty of 0.2 UI.**

***Index Terms*—CMOS integrated circuits, optical receivers, optical transmitters.**

I. Introduction

While multimode VCSEL-based interconnects currently dominate short-reach optical links (<100 m), silicon photonics is a strong candidate for longer distance applications typically found in data centers (up to 2 km). Silicon photonics incorporating WDM promises very high-bandwidth transceivers that may also satisfy the low-power and low-cost requirements of the datacom industry. Different implementations of silicon photonics are currently under investigation. In the monolithic integration paradigm, the electronics and the photonics share the same silicon wafer, enabling very low parasitics, and potentially a denser footprint than discrete solutions. However, there are some tradeoffs in tuning the fabrication process for best electronic or photonic device performance. For example, photonics wants thicker silicon to get a lower waveguide aspect ratio and tighter bend radius, while FETs want thinner silicon to get better gate control over channel and a smaller partially depleted region. Also, current monolithic processes have achieved integration with >100 nm [1] and sub-100 nm CMOS [2], but migrating or scaling the technology to new CMOS node is not necessarily straightforward and typically requires significant investment. In the hybrid integration paradigm, the electronics and the photonics are designed and fabricated on different platforms. This two-chip approach enables higher flexibility in choosing the best performance devices, with a potential disadvantage of higher interconnect parasitics between the chips. These effects can however be mitigated by using short wire-bonds or by flip-chip bonding the TX and RX drivers on the photonics. Using the hybrid approach, advanced CMOS technology can be used to drive silicon photonics components enabling low-power and high-speed transceiver modules. For instance, in [3], the authors demonstrated a fully integrated link at 10 Gb/s using 40 nm CMOS chips driving a ring modulator and a waveguide photodetector (PD) with a power efficiency of 2.1 pJ/bit, excluding laser wall-plug efficiency.

The flexibility offered by hybrid integration also enables more options for the design and fabrication of the photonics elements. Among these is the possibility to utilize III–V material as a gain medium on the silicon photonic platform. This approach, referred to as heterogeneous integration, was originally developed by groups at Ghent University [4], the University of California Santa Barbara [5], and Intel [6]. The heterogeneous platform enables low-loss and dense footprint silicon waveguides for all passive functions including waveguide routing, polarization handling and WDM filters. The integrated III–V material can be used to implement efficient modulators [7] and detectors [8] and to provide on-chip gain for lasers and semiconductor optical amplifiers (OAs). Having the laser source integrated on-chip is a main advantage of this architecture and there have been various demonstrations of heterogeneous lasers having performances comparable with InP-based devices [9], [10].

We present an optical link at 1.31 μm comprised of electroabsorption modulator (EAM) and PD devices hybrid integrated with low-power 32 nm CMOS electronics. The photonic devices were fabricated in a heterogeneous process using wafer-bonding

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N. Dupuis, B. G. Lee, J. E. Proesel, A. Rylyakov, C. W. Baks, and C. L. Schow are with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, USA (e-mail: ndupuis@us.ibm.com; bglee@us.ibm.com; jonproesel@us.ibm.com; sasha@us.ibm.com; cbaks@us.ibm.com; cschow@us.ibm.com).

R. Rimolo-Donadio was with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, USA. He is now with the Costa Rica Institute of Technology (ITCR), Cartago 30101, Costa Rica (e-mail: rrimolo@itcr.ac.cr).

A. Ardey was with the IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, USA. He is now with the College of Optics & Photonics (CREOL), University of Central Florida, Orlando, FL 32816-2700, USA (e-mail: aardey@us.ibm.com).

A. Ramaswamy, J. E. Roth, R. S. Guzzon, B. Koch, D. K. Sparacin, and G. A. Fish are with the Aurrion Inc., Goleta, CA 93117, USA (e-mail: anand.ramaswamy@aurrion.com; jon.roth@aurrion.com; rob.guzzon@aurrion.com; Brian.Koch@aurrion.com; daniel.sparacin@aurrion.com; greg.fish@aurrion.com).

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techniques to integrate III–V materials on silicon-on-insulator (SOI) wafers. We previously demonstrated in [11] data-rates up to 30 Gb/s, and have also shown transmission at 25 Gb/s over 10 km of single-mode fiber without penalty, highlighting the ability of silicon photonics to enable the reach needed for datacenters. In this paper, we present more details on the design and performance of the TX and RX assemblies and also show additional results of transmission experiments. The paper is organized as follows. In Section II we describe the heterogeneously integrated photonic devices. In Section III we present the TX and RX assemblies. In Section IV we present the results on the optical link. Finally, we conclude the paper in Section V

II. Heterogeneously Integrated Photonic Devices

The photonic devices used in the link were fabricated using III–V material heterogeneously integrated with silicon waveguides. They include an EAM and a waveguide PD. Both devices were fabricated using an established foundry infrastructure with Aurrion's heterogeneous integration process. The basic underlying photonic circuit is comprised of low-loss silicon and dielectric waveguides and is generated on an 8" SOI substrate. Heterogeneous integration of InP is realized by bonding "chiplets" of custom unprocessed InP epitaxial material to the silicon substrate. Subsequent lithography and etch steps are used to form a number of devices including lasers, OAs, modulators, and PD devices. Evanescent mode converters provide a conduit between the silicon and InP layers to optimally place the optical mode within the device structures. Further deposition and etch processing steps encapsulate the InP device structures with dielectric materials and form metal interconnects and contacts for interfacing with driver and control circuitry.

A. Electroabsorption Modulator

Fig. 1(a) shows the transmission spectra of the EAM for different bias voltages using TE-polarized light from a tunable external-cavity laser. The spectra were normalized to the transmission losses of a passive silicon waveguide. Far from the band edges, the intrinsic insertion loss of the EAM without bias is ~ 1 dB. With increasing voltage, the absorption edge shifts to longer wavelengths due to the quantum-confined Stark effect. The EAM can operate over a large wavelength range of $\sim$30 nm (see gray area in Fig. 1) while providing an extinction ratio (ER) larger than 20 dB with residual absorption below 3 dB. Fig. 1(b) presents the electro-optical (EO) small-signal response of the EAM (S_{21}, left axis) and the real part of S_{11} (right axis). For this measurement, the EAM was driven directly by a network analyzer (Agilent N5230A 40 GHz PNA) with no additional driver. A bias tee was added and the EAM was probed with GSG probes. The output light was coupled into fiber and a 40 GHz bandwidth u2t PD was used for optical to electrical conversion. The cables, the bias tee, and the probe were calibrated out. The EO S_{21} shows a 3-dB RC roll-off of 16 GHz that matches the purely electrical measurement, $\Re\{|S_{11}|\}$, and gives a capacitance of 200 fF at a reverse bias of 5.4 V. It should be noted that the EO bandwidth measurement is not a true measurement of the device speed but rather a way to measure its capacitance.

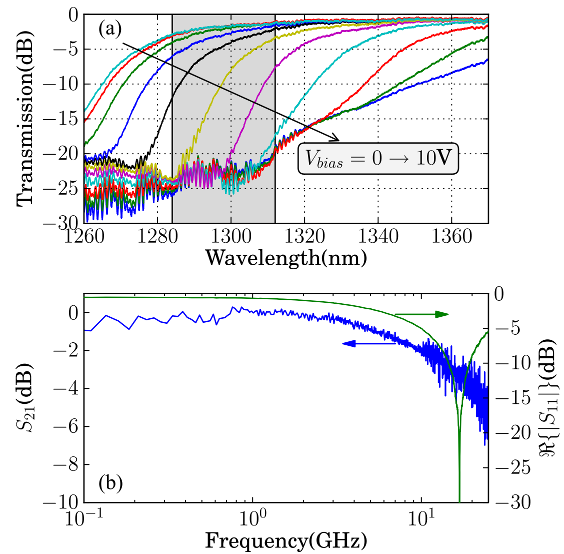

Fig. 1. (a) EAM transmission spectra for different reverse bias from 0 to 10 V (1 V steps); (b) EO and EE small-signal response of the EAM at a reverse bias of 5.4 V: S_{21} at 1310 nm (left axis), and $\Re\{|S_{11}|\}$ (right axis).

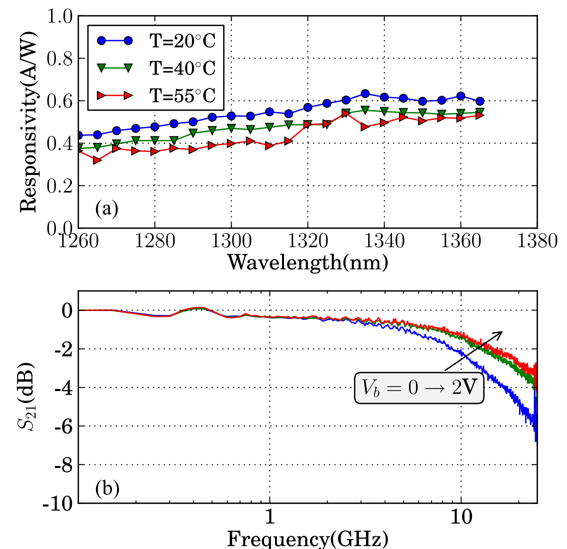

Fig. 2. (a) Responsivity spectra of the PD for different temperatures. (b) OE small-signal response of the PD for 0, 1 and 2 V reverse bias.

The EAM is essentially a capacitor which is here driven with a 50 Ω source. In the link presented below, the EAM is driven with a custom driver chip designed to deliver maximum amplitude to the capacitive load thus avoiding fixed impedance transmission lines.

B. Waveguide Integrated Photodiode

The *pin* PD structure is similar to that reported in [12]. In Fig. 2(a), we plot the internal responsivity (taking into account ~ 7 dB coupling losses) of the PD for different wavelengths and temperatures at a 1.5 V reverse bias. At 20 °C and 1310 nm, the responsivity is 0.55 A/W. The dark current of the PD

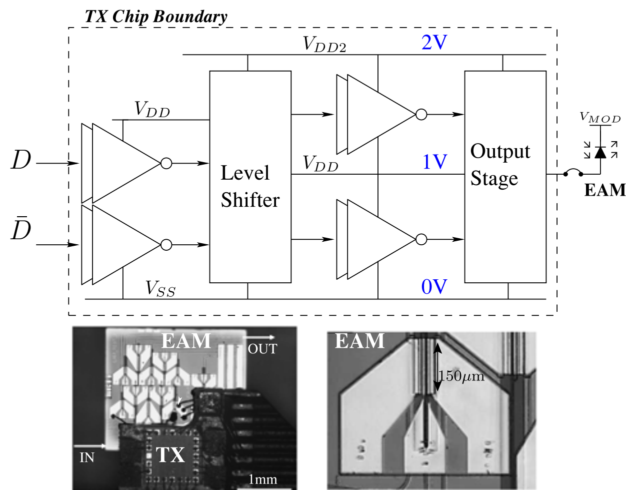

Fig. 3. TX block diagram (top) and pictures of the TX assembly (bottom) showing the wired-bonded package and a close-up of the EAM.

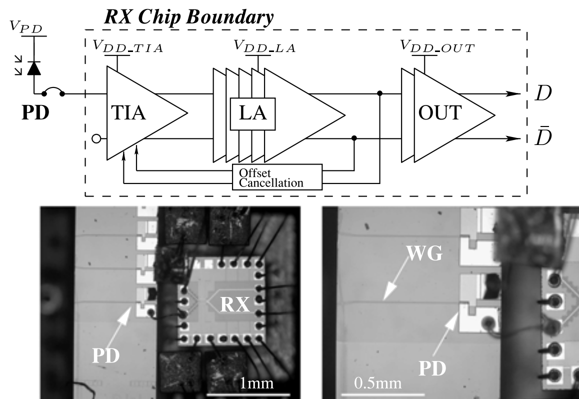

Fig. 4. RX block diagram (top) and pictures of the RX assembly (bottom) showing the wired-bonded package and a close-up of the PD.

was ~ 6 nA at a reverse bias of 1.5 V. In Fig. 2(b), we present the OE small-signal response of the PD. For that measurement, we used a lightwave component analyzer (Agilent N4373A 67 GHz LCA), and we calibrated down to the probe tips using an impedance standard substrate. As seen in the spectrum, the PD device exhibits a 3-dB bandwidth of 22 GHz at 2 V reverse bias.

III. Transmitter and Receiver Assemblies

In Figs. 3 and 4 we present high-level block diagrams illustrating the TX and RX assemblies used for the optical link. The TX consists of a driver chip wire-bonded to an EAM. The differential electrical inputs have 50 Ω on-chip terminations to $V_{\mathrm{DD}}/2$, followed by CMOS inverters to amplify the signal to full-swing CMOS levels. Cross-coupled CMOS inverters minimize timing error between the differential signals. The level shifter [13] provides low (V_{SS} to V_{DD}) and high (V_{DD} to V_{DD2}) CMOS outputs, which are buffered by inverter chains to drive the output stage [14]. The output stage uses cascoding to limit the static voltage across any device to V_{DD} while providing V_{SS} to V_{DD2} output swing [14], [15]. Using this stacked approach, we were able to provide an output swing of 2 V_{pp} to the EAM. The RX chip was reported previously in [16]. The RX consists of a PD wirebonded to the RX chip containing a transimpedance amplifier (TIA), a limiting amplifier (LA), an offset cancellation loop, and a 50 Ω output buffer (OUT). The combination of TIA, LA, and LPF has 39.1k Ω gain, 23.7 GHz bandwidth, 2.6 MHz low frequency cutoff, and 3.7$\mu\mathrm{A_{rms}}$ input-referred current noise in simulation after layout parasitic extraction. Both TX and RX were fabricated in IBM's standard 32 nm SOI CMOS technology, using thin oxide 1V breakdown devices only. The TX and RX circuits occupy 18 μm $\times$ 69 μm and 114 μm $\times$ 88 μm respectively. Both TX and RX sites were wirebonded to a high-speed custom PCB for testing. The PCB has short uncoupled 50 Ω traces for applying/extracting the high-speed differential signals to/from the TX/RX. Power and control biases are routed to wirebond pads near the chip and surface-mount decoupling capacitors are used on all the supplies. The PCB is cut into a diving board configuration for edge-coupled optical access.

IV. Optical Link Testing and Results

A. Experimental Setup

Fig. 5(a) describes the link setup which includes: a 1.31 μm commercially available DFB laser with an output power of 12 dBm, a polarization controller (PC), the TX assembly, an O-band OA with 20-dB gain, a fiber spool, a variable optical attenuator, another PC and the RX assembly. The output of the RX was connected either to a bit error rate (BER) tester or to a 50-GHz sampling scope. For all link measurements, the reverse bias on the EAM was fixed at 5.4 V and we measured a dynamic ER of ~8 dB with the 2 V_{pp} output swing of the CMOS driver. The reverse bias on the PD was 1.5 V. The photonics chips were accessed via lensed fibers using piezo-controlled stages. The optical power breakdown of the link was as follows: $\sim$21 dB EAM loss including 2$\times$ $\sim$7 dB coupling loss and $\sim$7 dB insertion losses (at 5.4 V reverse bias), and $\sim$7 dB coupling loss at the PD. The high coupling losses of the photonic devices are due to the absence of fiber couplers in the current designs and explain the need for an OA to close the link.

B. Results and Discussions

Fig. 5 presents the results of the link. In Fig. 5(b) and (c) we show optical and electrical eyes at 10, 20, 25 and 30 Gb/s data rates. The optical eyes were captured after the OA using the sampling scope optical head having a 30 GHz bandwidth and the optical power was ~0 dBm. The ringing observed on the transmitter eyes is attributed to wirebond inductance in the EAM to chip connection and is particulary noticable at 20 Gb/s. This ringing could be mitigated by optimizing the transmitter package using shorter wirebonds or by flip-chipping the driver chip onto the photonic device. The RX filters out the ringing as seen in the eyes of Fig. 5(c). Fig. 5(d) presents the measured RX sensitivity characteristics of the link for different data-rates. For the sensitivity measurements, the received power was referenced

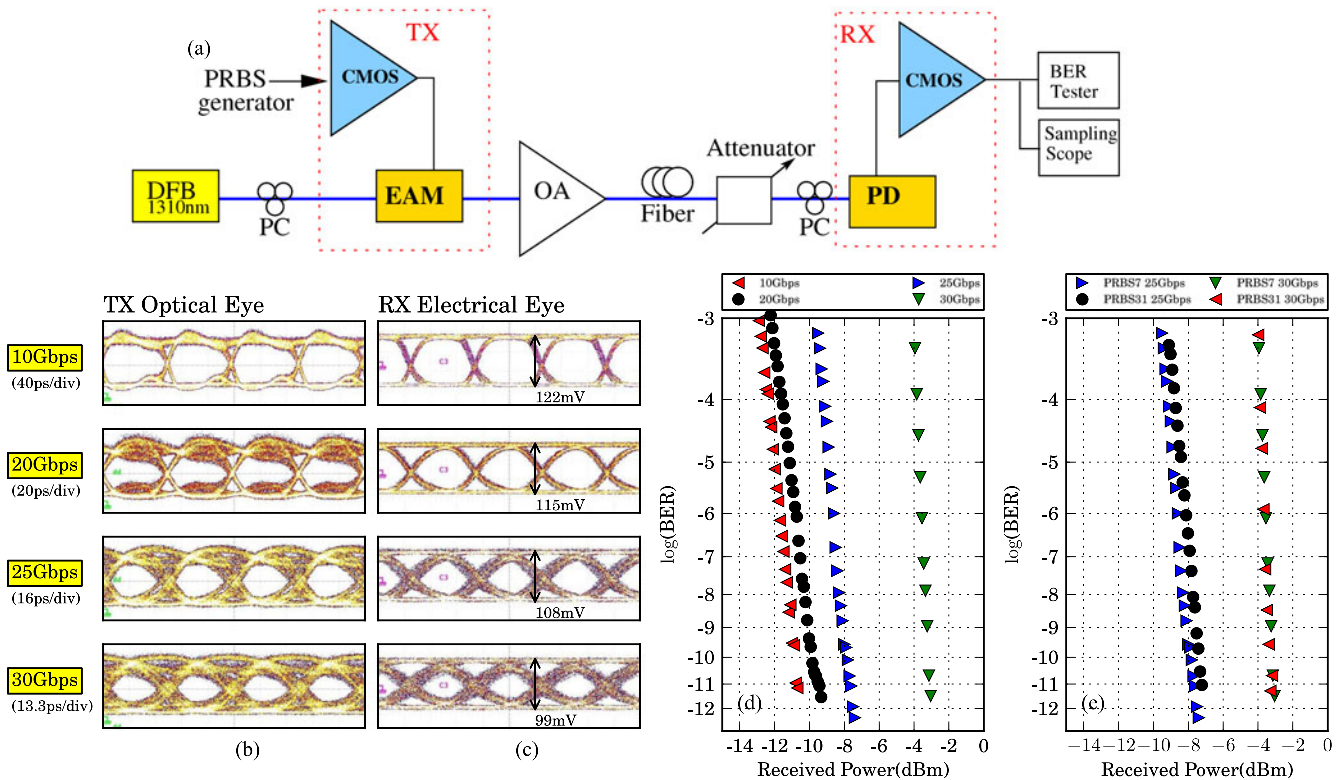

Fig. 5. (a) Experimental setup for high-speed link characterization; (b) Optical eyes captured after the transmitter at 10, 20, 25, and 30 Gb/s; (c) RX electrical eyes at 10, 20, 25, and 30 Gb/s; (d) RX sensitivity of the link at 10, 20, 25, and 30 Gb/s for PRBS7; (e) RX sensitivity of the link at 25 and 30 Gb/s for PRBS7 and PRS31. For the sensitivity measurements the received power was referenced to the light coupled in the silicon waveguide and corrected for infinite extinction ratio.

to the light coupled in the silicon waveguide through received photo-current and corrected for infinite ER. At BER=10^{-12}, the RX sensitivity was −10.5, −9.4, −7.6, and −3.2 dBm at data-rates of 10, 20, 25, and 30 Gb/s, respectively. Negligible sensitivity degradation was observed when moving from $2^7 - 1$ PRBS to $2^{31} - 1$ PRBS at 25 and 30 Gb/s as seen in Fig. 5(e). In Fig. 6(a) we present the sensitivity curves at 25 Gb/s after 11 km of fiber transmission and show no measured penalty compared with the back-to-back curve. The bathtub curves in Fig. 6(b) indicate small closure of the eye (∼0.2UI) when moving from back-to-back to 11 km fiber transmission, likely due to the dispersion of the fiber. We used two different transmitters for the measurements described above. The two assemblies were packaged in exactly the same manner using nominally identical chips and we did not observe any differences in the link sensitivity under identical conditions. A first version was used for the sensitivity measurements at 10, 20, and 25 Gb/s PRBS7, and a later version was used for 30 Gb/s PRBS7, PRBS31 measurements and all transmission characterizations. The eyes were also captured with the later version.

We used similar power settings for all measurements and measured a power efficiency (excluding laser and amplifier) of 3 pJ/bit at 30 Gb/s. This includes 1.25 pJ/bit for the TX assembly and 1.75 pJ/bit for the RX assembly. The power efficiency can likely be improved at lower data-rates at the expense of the bandwidth of the RX as shown in [16]. The external OA was necessary to offset the high coupling losses of both EAM and PD chips which did not have fiber couplers to efficiently transition

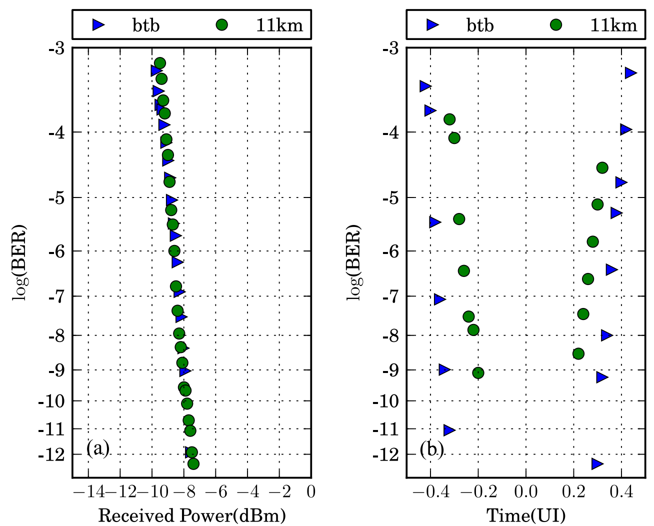

Fig. 6. Transmission experiment at 25 Gb/s and PRBS7; (a) link sensitivity and (b) bathtub curves in back-to-back and after 11 km of fiber transmission.

the optical mode between the waveguide and the fiber. If fiber mode converters were included and the coupling losses were (conservatively) reduced to 3 dB per facet, the link without amplifier would have ∼3 dB margin at 25 Gb/s assuming the same laser input power of 12 dBm and a RX sensitivity of −7.6 dBm [see Fig. 5(e)]. This margin could be further improved by

integrating the laser on-chip which is a significant advantage of the heterogeneously integrated approach [9].

V. Conclusion

We presented an optical link combining fast and efficient heterogeneously integrated silicon photonics with 32 nm CMOS electronics. We demonstrated data-rates up to 30 Gb/s and transmission at 25 Gb/s over more than 10 km of fiber with no penalty. We measured a power efficiency of 3 pJ/bit excluding the laser and the OA. By including fiber couplers into the photonic components, we expect to be able to close the link with $\sim$3 dB margin at 25 Gb/s with further potential improvement enabled by monolithic integration of the laser with the EAM. Our results illustrate the potential speed and efficiency offered by combining high performance heterogeneously-integrated photonics with advanced CMOS to meet the challenging requirements of next-generation data centers.

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Nicolas Dupuis received the B.S. and M.S. degrees from Université Blaise Pascal, Clermont-Ferrand, France, and the Ph.D. degree from Université de Lorraine, Metz, France, in 2009, all in physics. He is currently a Postdoctoral Researcher at the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA. His research interests include silicon photonics, optical switching and optical link modeling. Before joining IBM, he was with Bell Laboratories, Crawford Hill, NJ, USA, working on high-speed InP-based photonic circuits.

Benjamin G. Lee (M’04–SM’14) received the B.S. degree from Oklahoma State University, Stillwater, OK, USA, in 2004, and the M.S. and Ph.D. degrees from Columbia University, New York, NY, USA, in 2006 and 2009, respectively, all in electrical engineering. In 2009, he became a Postdoctoral Researcher at IBM Thomas J. Watson Research Center, Yorktown Heights, NY, where he is currently a Research Staff Member. He is also an Assistant Adjunct Professor of electrical engineering at Columbia University. His research interests include silicon photonic devices, integrated optical switches and networks for high-performance computing systems and datacenters, and highly parallel multimode transceivers. Dr. Lee is a member of the Optical Society and the IEEE Photonics Society, where he serves as an Associate Vice President of Membership. He serves on the technical program committees for the Optical Fiber Communications Conference and the Optical Interconnects Conference.

Jonathan E. Proesel (M’10) received the B.S. degree in computer engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 2004. He received the M.S. and Ph.D. degrees in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 2008 and 2010, respectively. He joined the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, in 2010, where he is currently a Research Staff Member working on analog and mixed-signal circuit design for optical transmitters and receivers. He has also held internships with IBM Microelectronics, Essex Junction, VT, USA, in 2004 and IBM Research, Yorktown Heights, in 2009. His research interests include high-speed optical and electrical communications, silicon photonics, and data converters. Dr. Proesel is a member of the IEEE Solid-State Circuits Society. He received the Analog Devices Outstanding Student Designer Award in 2008, the SRC Techcon Best in Session Award for Analog Circuits in 2009, and co-received the Best Student Paper Award for the 2010 IEEE Custom Integrated Circuits Conference.

Alexander Rylyakov received the M.S. degree from the Moscow Institute of Physics and Technology, Moscow, Russia, and the Ph.D. degree from State University of New York at Stony Brook, Stony Brook, NY, USA, both in physics. He is a Research Staff Member at the IBM T.J. Watson Research Center, Yorktown Heights, NY. His current research interests include high-speed integrated circuits for optical communications and high-performance digital phase-locked loops.

Renato Rimolo-Donadio (S'08–M'11) received the B.S. and Lic. degrees in electrical engineering from the Technical University of Costa Rica (ITCR), Cartago, Costa Rica, in 1999 and 2004, respectively, the M.S. degree in microelectronics and microsystems, and the Ph.D. degree in electrical engineering, both from the Technical University of Hamburg-Harburg (TUHH), Hamburg, Germany, in 2006 and 2010, respectively. In 2014, he joined as a Professor at the Electronics Engineering Department, Instituto Tecnolgico de Costa Rica (ITCR). From 2012 to 2014, he was with the IBM T.J. Watson Research Center, and from 2006 to 2012, with the Institute of Electromagnetic Theory, Technical University of Hamburg-Harburg. His current research interests include system-level modeling and optimization of interconnects, analysis of signal and power integrity problems, and high-speed circuit design.

Christian W. Baks received the B.S. degree in applied physics from Fontys College of Technology, Eindhoven, The Netherlands, in 2000 and the M.S. degree in physics from the State University of New York, Albany, NY, USA, in 2001. He joined the IBM T.J. Watson Research Center, Yorktown Heights, NY, as an Engineer in 2001, where he is involved in high-speed optoelectronic package and backplane interconnect design specializing in signal integrity issues.

Abhijeet Ardey received the M.S. degree in physics from the University of Delhi, Delhi, India, in 2003 and the M.S. and Ph.D. degrees in physics from the University of Central Florida (UCF), Orlando, FL, USA, in 2007 and 2014, respectively. He is currently a Research Scientist at CREOL, The College of Optics and Photonics, at UCF. His research interests include the development of novel low-noise modelocked semiconductor lasers and integrated devices for applications in future high-capacity optical communication networks.

Clint L. Schow (SM'10) received the Ph.D. degree in electrical engineering from the University of Texas at Austin, Austin, TX, USA, in 1999. He joined IBM, Rochester, MN, USA, assuming responsibility for the optical receivers used in IBMs optical transceiver business. From 2001 to 2004, he was with Agility Communications, Santa Barbara, CA, USA, developing high-speed optoelectronic modulators and tunable laser sources. In 2004, he joined the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, as a Research Staff Member and currently manages the Optical Link and System Design Group responsible for optics in future generations of servers and supercomputers. He has directed multiple DARPA-sponsored programs investigating chip-to-chip optical links, nanophotonic switches, and future systems utilizing photonic switching fabrics. He has published more than 150 journals and conference articles and has 16 issued patents. Dr. Schow is a senior member of the OSA.

Anand Ramaswamy received the B.S. degree in electrical engineering with a minor in physics and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, CA, USA, and the University of California, Santa Barbara, Santa Barbara, CA, in 2005, 2007, and 2010, respectively. He is currently the Photonics Systems Manager at Aurrion Inc., Santa Barbara. His current research interests include photonic integrated circuits for optical communications.

Jonathan E. Roth was born in Lansdale, PA, USA, in 1977. He received the B.S. degree in biomedical engineering from Case Western Reserve University in Cleveland, OH, USA, in 2000, and the Ph.D. degree in electrical engineering from Stanford University in Stanford, CA, USA, in 2007. His dissertation work was on electroabsorption modulators in indium phosphide and silicon germanium. He is employed by Aurrion Inc. as a Senior Optoelectronic Device Engineer, where he designs heterogeneous III–V on silicon devices and photonic integrated circuits.

Robert S. Guzzon received the B.S. degrees in electrical engineering and physics from Lehigh University in Bethlehem, PA, USA, in 2007 and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Santa Barbara, CA, USA, in 2011 where his dissertation focused on the theory, design, and fabrication of high-SFDR photonic integrated microwave filter circuits. His current interests include the development of photonic integrated circuit systems and their electronic and optical interfaces.

Brian Koch received the B.S. degree in physics (Hons.) from the College of William and Mary, Williamsburg, VA, USA, in 2003 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, Santa Barbara, CA, USA, in 2004 and 2008, respectively. His dissertation was focused on optoelectronic resonators and mode-locked lasers in photonic integrated circuits, with applications in optical clock recovery and optical signal regeneration. He is a Design Engineering Manager at Aurrion. He has been heavily involved in the development of heterogeneous silicon laser technology for more than seven years. He was an Optical Researcher at Intels Photonics Technology Lab in Santa Clara, CA, from 2008 to 2012, where he was involved in the design and testing of heterogeneously integrated silicon lasers and other silicon-based photonic components and circuits. Since joining Aurrion in 2012, he has has been with a design team developing novel devices and architectures on a silicon-based heterogeneous integration platform. Dr. Koch holds two patents and has authored more than 40 papers and two book chapters.

Daniel K. Sparacin (M'12) received the B.S. degree in material science and engineering from Brown University, Providence, RI, USA, in 2000 and the Ph.D. degree from MIT, Cambridge, MA, USA, in 2006 focused on silicon photonics device design and fabrication. After graduation, he consulted for Defense Advanced Research Projects Agency Microsystems Technology Office in the areas of digital and RF photonic materials, devices, and systems. In 2012, he joined Aurrion, Goleta, CA, USA, where he is the Director of Technology.

Greg A. Fish (SM'11) received the B.S. degree in electrical engineering from the University of Wisconsin at Madison, Madison, WI, USA, in 1994 and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 1999. He is the Chief Technology Officer at Aurrion, Goleta, CA, USA. He is considered as a Leading Expert in the field of photonic integration with nearly 20 years of experience in the field of InP-based photonic integrated circuits. He is an author/coauthor of more than 60 papers in the field and has 12 patents.