A Simple Approach for the Design of Operational Transconductance Amplifiers for Low Power Signal Processing

Alfonso Chacón-Rodríguez
Escuela de Ingeniería Electrónica
Instituto Tecnológico de Costa Rica
Apartado Postal: 159-7050, Cartago 30101, Costa Rica
Email: alchacon@itcr.ac.cr

Santiago Sondon
Pablo Mandolesi†
Pedro Julián*
GISEE
Universidad Nacional del Sur
Alem 1253, Bahía Blanca, Argentina
Email: {ssondon, pmandolesi}@uns.edu.ar
pjulian@ieee.org

***Abstract*—A simple approach for the design, fabrication and characterization of a operational trasconductance amplifier intended for work in low power applications is reported in this work. DC Measured parameters agree with simulation results and specifications. An application for the designed OTA is also tested.**

I. Introduction

As it has been reported extensively on literature, linearized transconductors find wide application in low power signal processing. In this case, a continuous Gm-C paralell filter bank, and several analog computing structures were to be build on a CMOS 0.5 μm process, in order to implement a continuous gunshot detector [1]. The signals to be processed have a required bandwidth of [100Hz, 1250Hz], and a maximum peak voltage swing of 550mV. The detector is intended for its use in surveillance wireless sensor network against illegal hunting in tropical forest reserve. As such, power consumption is critical and each component must be adequately sized.

Usually, most of the available equations and relationships used for the design of transconductors are based on the long channel quadratic equations [2], [3], though there are some approximations in the literature to the design of OTAs using the weak inversion models of the transistor [4]. And while there is also plenty of literature on the design of OTAs and operational amplifiers [5]–[8], as well as other complex structures [9], [10], using the EKV or the ACM MOSFET models, there is nonetheless scarce material on a similar design approach for standard linearized transconductors.

We propose in this paper a simple approach for the design of the ubiquitous Krummenacher's linearized CMOS OTA [11], with equations derived from the EKV model, and show an example of its implementation. The paper is organized as follows: Section II presents the general process used for the design of an OTA intended for low power applications. Section III presents a case study of a particular design and its simulation results. Section IV presents measurements of the case study. Finally, Section V concludes the paper and discuss the oncoming work.

II. Design Process of an Operational Transconductance Amplifier

A typical linearized OTA, as proposed by Krummenacher in [11] and shown in Fig. 1, has an optimum size relation of 6.7 between the sizes of the difussor and the input differential transistor pairs. This relation is derived directly from the long channel MOS quadratic equations. In [4], an alternative relation of 2 is derived, when the transistors are to be operated in the weak inversion region. In the first case, the total OTA G_m equals approximately 4.7 times the input transistor's g_m, while in the second case, this relation is of approximately 3. In our case, the OTA's slew rate and power requirements implied transistors working near the moderate inversion region, but with a linearized G_m characteristic with an input range of at least $1V_{pp}$. To avoid a tiresome simulation approximation, an analytic expression for the equivalent transconductance was derived from the EKV model [12]. From these equations, using Krummenacher's optimum transistor relation, an expected OTA G_m can be obtained in terms of the transistors' g_m, if the transistors are taken from the moderate inversion region towards the strong inversion zone.

If K is the OTA's transconductance in terms of the input transistors' g_m, then

$$G_m \approx \frac{gm_{M_1}}{K} \tag{1}$$

Analitically, G_m can be expressed as (see [13]):

$$G_m \approx \frac{gm_{M_1}}{2 + \frac{gm_{M_1}}{2gm_{M_2}}} \tag{2}$$

*P. Julián is member of Consejo Nacional de Investigaciones Científicas y Técnicas CONICET, Av. Rivadavia 1517, Buenos Aires, Argentina.

†P. Mandolesi is member of CIC (Comisión de Investigaciones Científicas), Pcia. Bs. As, La Plata, Argentina.

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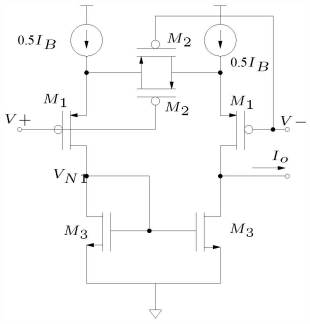


Fig. 1. PMOS Krummenacher's OTA. PMOS input transistor are chosen due to their intrinsic lower transconductance.

If one considers that

$$gm_{M_1} = \frac{I_{BIAS}}{n\phi} G_{i_{f1}} \tag{3}$$

with $G_{i_{fx}}$ the normalized transconductance x in terms of the maximum transconductance, Eq. (2) may be re-written as

$$G_m \approx \frac{gm_{M_1}}{2 + \frac{G_{i_{f1}}}{2G_{i_{f2}}}} \tag{4}$$

If transistor M_2 is scaled in terms of M_1, and assuming both biased with the same current, then M_2 may end up in a different inversion region than M_1. Following the EKV basic equations [12], one may define inversion currents i_{f1} e i_{f2} for each transistor. Since

$$i_{f_x} = \frac{I_{BIAS}}{I_s \frac{W_x}{L_x}} \tag{5}$$

with

$$I_s = \mu C_{ox} n \phi^2 \tag{6}$$

the specific current for the process, and using the aspect relation between the transistors, then

$$\frac{g_{M_1}}{2g_{M_2}} = \frac{\sqrt{1 + 0.5\sqrt{7}\sqrt{i_{f1}} + 7i_{f1}}}{\sqrt{1 + 0.5\sqrt{i_{f1}} + i_{f1}}} \tag{7}$$

Solving this equation, one can then find out the wanted transconductance relation

$$K = 2 + \frac{g_{M_1}}{2g_{M_2}} \tag{8}$$

Intuitively, one can verify that, for $i_{f1} \ll 1$, $K \approx 3$, whereas if $i_{f1} \gg 1$, $K \approx 4.64$. Both values verify Eq. (2) when the transistors are in the weak inversion region (where $gm_{M_1} \approx gm_{M_2} \approx I_{BIAS}/n\phi$), and the well known relation when they are in the strong region zone (see [13]). Figs. 2 y 3 show the variation of $K = G_m/g_m$ in terms of the normalized transistor transconductance $G(i_f)$ and its inversion level i_f, as defined by the EKV model.

III. Case Study

The goal was to design a paralell filter with three specific pass-bands: [875Hz,437Hz], [437Hz,219Hz] and [219Hz,109Hz]. Since 875Hz was the top 3dB cutoff frequency, and the chosen sizes of the capacitors where in the order of 25pF to 50pF, a slew rate of 2.75 mV/μs was specified as the starting point for the design. This particular slew rate implied a minimum bias current of almost 70nA, that was taken to 90nA to account for possible extra parasitic capacitances or peak signals a little above the expected 500mV.

Simulations with arbitrary transistor sizing but following Krummenacher's 6.7 size ratio showed that placing the transistors from the moderate too much towards the weak inversion zone ruined the linearization, as the diffusors were taken from the triode into the saturation region when the input differential voltage approached zero. Using a smaller transistor ratio solved the issue, at the cost of a smaller linear zone, as already shown in [4]. The compromise was found by choosing always moderate inversion, but slightly into the strong inversion zone, with a i_f of 3 to 4 and a final normalized transconductance between a 40% to 35% of the maximum one ($G_{i_f} \approx 0.4 * I_D/nV_T$) [12].

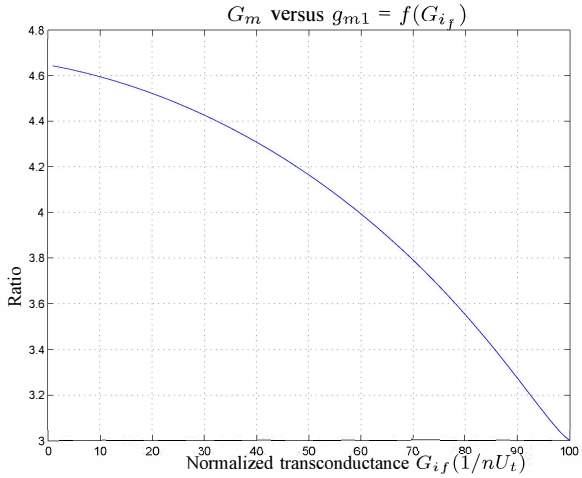


Fig. 2. Ratio between the OTA transconductances and the input transistors' $K = gm_{M1}/G_m$, as a function of the normalized transistors' transconductance $f(G_{i_f})$.

A basic 137nS OTA was designed to provide for the top cutoff frequency. The rest of the cutoff frequencies were to be obtained by scaling this transconductor using the current division technique proposed in [5], and by adding or substracting the corresponding capacitor sizes. A Matlab script containing the derived equations was used for the sizing of the transistors in terms of the expected transconductance, using as input parameters the bias current and the intended inversion level. If the transistor length parameter was used as an input as well, the script provided then with information about the parasitic capacitances resulting from the calculated transistor sizes. Results were then checked against an Eldo

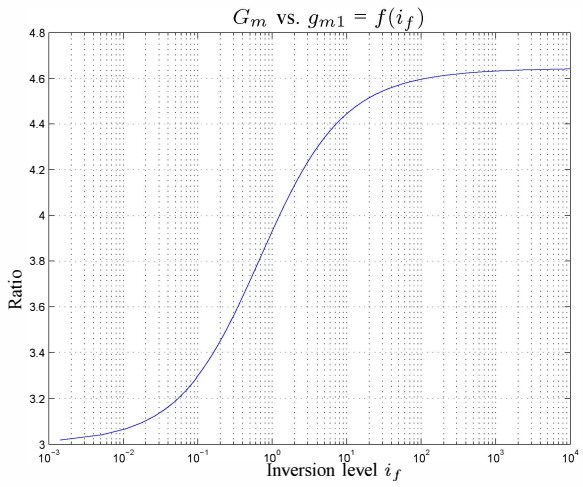


Fig. 3. Ratio between the OTA transconductances and the input transistors' $K = gm_{M1}/G_m$, as a function of M_1 inversion level i_f.

spice simulation, approximating the required sizes by a series-parallel association of unitary transistors. These unitary transistors were all long channel ones chosen with sizes as close as possible to those used by the foundry to generate their BSIM models. Simulations also allowed for a confirmation of the expected linear range. As a whole, it took no more than a few iterations to obtain the definitive transistor sizes. Transconductance simulation results are shown in Fig. 4.

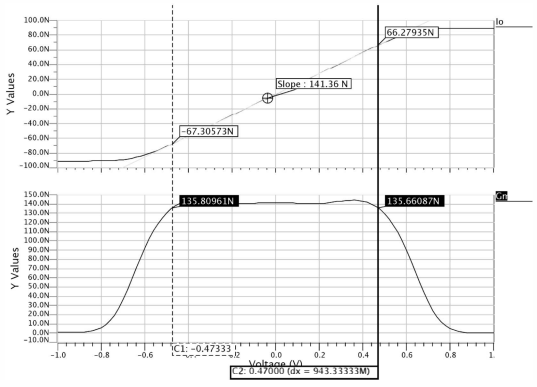


Fig. 4. Simulation of OTA's output current and transconductance.

The layout technique used was proposed in [5], [14]. Here, input and diffusor transistors are piled up and intermixed, to improve matching. An example for a 34nS OTA is shown in Fig. 5, where the final transconductance is obtained by dividing the input's 137nS by a factor of four, using the aforementioned current division technique. An IC with the intended paralell filter bank was designed using the Mentor Graphics environment, but leaving aside a single 137nS OTA structure for its separate characterization.

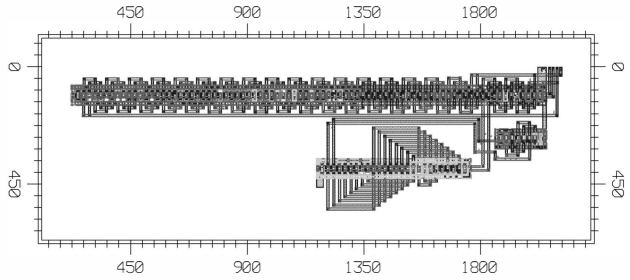


Fig. 5. Layout example. In this case, a 34.25nS OTA, based on a 137nS input OTA, with its transconductance scaled down by current division [5]. Input and diffusor transistors, as well as the division mirror ones are piled up and intermixed using the technique proposed in [5], [14]

IV. Measurements

For DC signal injection and measurement an Agilent E5270B framework with E5287A modules was used. Instruments were operated remotely through a GPIB bus with a computer runing a script in MatLAB. The tested OTA had a regulated input bias, to adjust its transconductance. V_{DD} was 4V. In Fig. 6 and Fig. 7 measured transference curve and calculated transconductance are shown respectively.

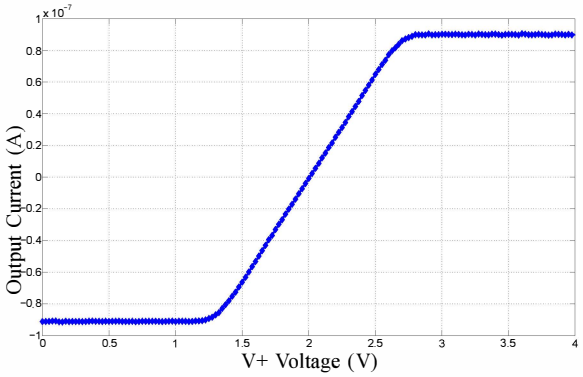


Fig. 6. Measured transference curve for OTA.

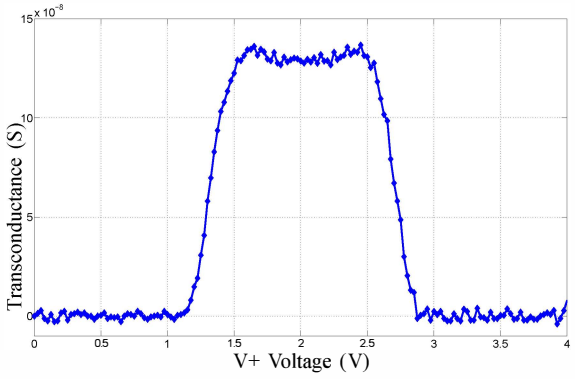


Fig. 7. Calculated transconductance curve for OTA.

Parameters extracted from measurements are shown on table I. Measurements evidence that for the intended 90nA input

current bias, the obtained transconductance has an error of 5% from the expected one. OTA's frequency response shows that gain and bandwith are well for the intended application.

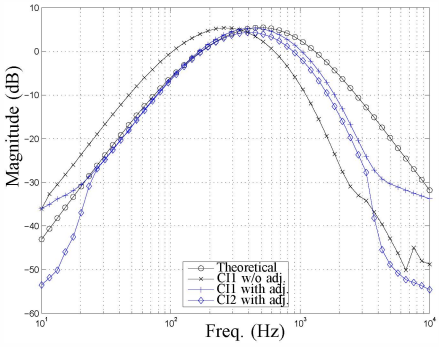
TABLE I
MEASURED OTA'S DC PARAMETERS

I1	I2	V-	Transconductance	Offset	Linear range
30 nA	30 nA	2 V	104 nS	4.6 mV	970 mV
45 nA	45 nA	2 V	130 nS	6.3 mV	1000 mV
45 nA	45 nA	1.75 V	132 nS	6.3 mV	1000 mV
45 nA	45 nA	2.25 V	132 nS	2.3 mV	1100 mV
60 nA	60 nA	2 V	152 nS	5.1 mV	1000 mV
40 nA	50 nA	2 V	129.6 nS	-45.7 mV	1000 mV

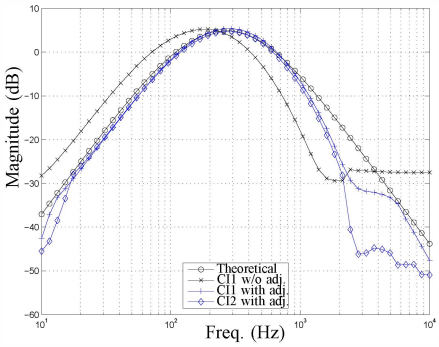
The AC response of the intended bank of filters, as implemented on two different IC's is shown in Fig. 8. The adjustable bias current of the OTAs allowed for a fine tuning of the cutoff frequencies, to compensate for capacitance and transconductance process deviations. Some extra adjustment was required due to the high input capacitance of some of the OTAs, that also produced a sharper roll off on the first bank. This deviation was nonetheless an effect of the chosen filter topology, and may be easily corrected. In general the design process of the OTAs showed to be fast and relatively precise.

V. CONCLUSIONS

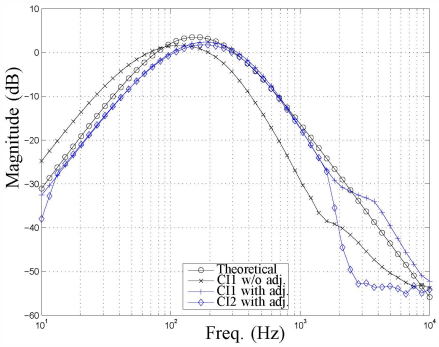
A simple method for the quick design of linearized OTAs working in the moderate inversion regime has been shown. The method has been tested with the implementation of various transconductors that have been used later as components of a Gm-C bank filter. Testing results of a particular OTA were within 5% of the expected transconductance, with a linear range of $1V_{pp}$ and a bias current of only 90nA.



(a) Bandpass filter (875Hz, 437Hz).



(b) Bandpass filter (437Hz, 219Hz).



(c) Bandpass filter (219Hz, 109Hz).

Fig. 8. Frequency response for a three bandpass parallel bank filter implemented with the designed OTAs (two IC's tested). The adjustable bias current of the OTAs allowed for a fine tuning of the cutoff frequencies, to compensate for capacitance and transconductance process deviations.

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