# Flexible Transmitter Employing Silicon-Segmented Mach–Zehnder Modulator With 32-nm CMOS Distributed Driver

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Abstract—We propose a flexible optical transmitter for the short-reach optical interconnects that includes a silicon photonic segmented Mach–Zehnder modulator driven by a distributed six-channel 32-nm silicon on insulator (SOI) complementary metal-oxide semiconductor driver integrated circuit. Optical equalization is demonstrated to extend the bandwidth limitation of the transmitter with non-return to zero signaling at 25 Gb/ s. We also generate four-level pulse amplitude modulation (PAM-4) signaling using the same transmitter architecture. Transmission of 46 Gb/s PAM-4 signal with bit error rate (BER) well below hard-decision forward error correction limit is experimentally demonstrated. Low driver power consumption of 130 mW at 46 Gb/s PAM-4, corresponding to 2.8 pJ/bit power efficiency, is also achieved.

*Index Terms*—Distributed driver, modulator, optical interconnects, silicon photonics.

#### I. INTRODUCTION

PTICAL interconnects targeting both short and long reaches in intra- and inter-datacenter networks, as well as access and metro networks, have recently received an increased interest due to the tremendous growth in data traffic [1]. To address this exponential growth, high bandwidth, energy efficient and low cost optical transceivers are needed. While today the short-reach optical interconnects (up to 300 m) deployed inside the datacenter are dominated by low cost VCSEL-based multimode-fiber links, there is a growing demand for longer reach optical links in intra- and inter-datacenter interconnects

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(from 500 m to 10 km) for datacenter expansion or installation of new mega-datacenters [2]. The use of single-mode fiber infrastructure operating at wavelengths in the 1.3  $\mu$ m transmission window for newly installed mega-datacenters, or interconnects between datacenters, open promising opportunities and also many challenges for silicon photonic integration. With the advantages of building on the long history of complementary metal-oxide semiconductor (CMOS) technology, silicon photonics would potentially provide a low cost, large scale integration, power efficient and small footprint solution [3], [4] to cope with the exponential increase in data traffic.

The modulator is a central device in optical transmitters and has attracted extensive research and development in both academia and industry over the last decade [5]. Here, we investigate a flexible transmitter which includes a co-packaged segmented MZM and a low power 32 nm CMOS multi-channel IC driver for the next generation of optical interconnects. The flexibility of the transmitter is brought about by the multi-segment approach in the design of the high-speed phase shifters. The transmitter first leverages the well-known advantages of segmented modulators, which reduce the device capacitance seen by each driver channel by breaking the long phase shifter into many short segments, enabling extended modulation bandwidth. The multiple segments can then be employed in various manners to provide maximum extinction ratio, to perform optical equalization (EQ), or to provide multi-level signaling. In the case of EQ, the bandwidth may be further extended using techniques such as feed-forward equalization (FFE). Although FFE can be generated by driving a segmented modulator with an equalized driver IC, typically this requires a linear driver with significantly more bandwidth than the modulator. Alternatively, the scheme that we first demonstrated in [6] provides equalization in the optical domain while using non-linear, un-equalized drivers. Moreover the transmitter can easily be used to migrate to higher order modulation formats such as multi-level pulse amplitude modulation (PAM), or can deploy adaptive-PAM modulation formats for dynamic optical networks.

Previously segmented MZM designs were reported on the silicon platform [7] and recently on the InP platform [8] for non-return to zero (NRZ) signaling. Higher order modulation formats generated by segmented modulators were also reported such as PAM-4 in [9], [10] and 64-Quadrature Amplitude Modulation (64-QAM) in [11]. In [6], we presented a transmitter

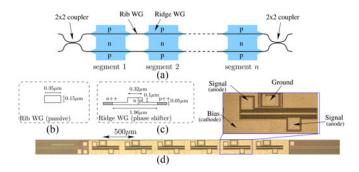


Fig. 1. Design and fabrication of the segmented modulator: (a) waveguide structure of the MZM; (b) cross-section of the rib waveguide and dimensions; (c) cross-section of the ridge waveguide and dimensions; (d) annotated die pictures of a segmented modulator having six 400  $\mu$ m-long segments on a 500  $\mu$ m pitch.

design using optical equalization and demonstrated improved BER performance of the optical link at 22 Gb/s. In this paper, we report more details on the transmitter fundamentals and design with extensive experimental results. Optical equalization performance at higher bitrates: a 25 Gb/s NRZ signal as well as BER performance of PAM-4 signals up to 46 Gb/s, is presented. The organization of the paper is as follows: Section II discusses the design of the silicon modulator and the driver IC employed in the flexible transmitter, Section III reports the experimental measurements and results for optical equalization of NRZ signaling, Section IV presents the experiments and BER performance of PAM-4 signaling, and finally, Section V concludes the paper.

## II. TRANSMITTER DESIGN

In this section, we describe the design of the flexible transmitter that includes a six-segment silicon MZM co-packaged with a six-channel 32 nm CMOS driver IC. The assembly of the device on a printed circuit board (PCB) is then presented.

#### A. Segmented Mach-Zehnder Modulator

The segmented Mach-Zehnder modulator was designed and fabricated in IBM developed CMOS Integrated Nano Photonics technology CMOS9WG [4]. The MZM has a  $2 \times 2$  structure using fully-etched silicon waveguides and  $2 \times 2$  input and output directional couplers. Both arms of the MZM are equipped with six modulator segments of either 300  $\mu$ m or 400  $\mu$ m and the pitch between the segments is 500  $\mu$ m. Each elementary segment has a ridge waveguide structure and implants on the partially etched silicon define a p-n diode, which is operated in carrierdepletion mode. More details on the p-n phase shifter structural parameters can be found in [12] and [13]. Each segment has rib-to-ridge and a ridge-to-rib waveguide transition tapers at the input and output respectively, in order to ensure a good electrical isolation between segments. The MZM also includes in each arm a 50  $\mu$ m-long resistive heater that consists of a thin silicide layer embedded within a ridge waveguide. Fig. 1 presents a schematic of the MZM waveguide structure (a) as well as cross-section of the rib (b) and ridge waveguides (c). Fig. 1(d) shows annotated die pictures of a segmented modulator

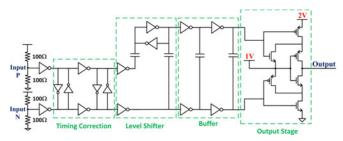


Fig. 2. Circuit schematic showing one 2-Vpp driver channel.

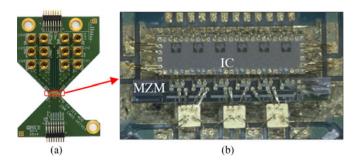


Fig. 3. (a) Custom printed circuit board and (b) micrograph of packaged segmented modulator with driver IC.

after fabrication having six 400  $\mu m$  segments. The measured capacitance of each segment was  $30\, {\rm fF}/\, 100\, \mu m$  and the pad capacitance was about 40 fF at a  $-3{\rm V}$  bias. The  ${\rm V}\pi\text{-L}$  of the phase shifter was 2.04 V-cm.

#### B. 32 nm CMOS Distributed Driver IC

The CMOS distributed driver IC is a 6-channel version of the IC reported in [14]. The spacing between each driver channel is 500  $\mu$ m, matching the pitch of the modulator segments. Fig. 2 shows the circuit design of one driver channel in the  $6 \times 1$ array. The RF inputs have 50  $\Omega$  terminations for impedance matching with standard laboratory equipment (in particular, the bit pattern generator output), followed by CMOS inverters to amplify the signal to 1 Vpp. Cross-coupled CMOS inverters minimize the timing error between the differential signals. A level shifter stage provides low (0 to 1 V) and high (1 to 2 V) CMOS outputs, which are buffered by inverter chains to drive the output stage. The output stage has a cascode configuration to limit the static voltage across any device to 1 V while providing 2-Vpp output swing. Each of the six driver circuits occupies  $60 \ \mu \text{m} \times 31 \ \mu \text{m}$ , for a total circuit area of  $0.011 \ \text{mm}^2$ . The driver IC is  $3.4 \text{ mm} \times 0.9 \text{ mm}$ .

#### C. Transmitter Assembly

The segmented MZM and 6-channel driver IC were wirebond co-packaged on a custom PCB as shown in Fig. 3(a). The PCB has cut-outs for input and output fibers, SMP connectors for high-speed drive signals, and two ribbon cable connectors for DC biasing. Decoupling capacitors are used for low-pass filtering of all of the DC power supplies. A zoom-in micrograph of the driver IC (upper) and the segmented MZM (lower)

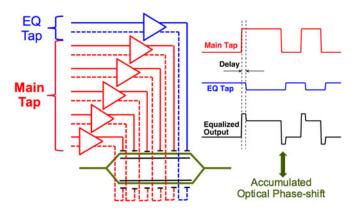


Fig. 4. Optical equalization with segmented MZM and multi-channel driver IC.

with decoupling capacitors for the modulator's cathode bias is illustrated in Fig. 3(b).

## III. OPTICAL EQUALIZATION WITH SEGMENTED MODULATOR

Optical FFE can be performed for NRZ signaling using the proposed transmitter design by simply employing one or more of the segments as equalizer taps. Fig. 4 illustrates the fundamental concept utilizing the segmented modulator in a two-tap EQ scheme. The EQ tap (shown in blue) is inverted and delayed with respect to the main tap (red). The tap weight can be discretely controlled by selecting the number of segments used for each tap, and can be in theory further optimized by adjusting the drive voltage or segment length of each tap independently. Compared with the electrical equalization implemented within the driver IC, this optical equalization scheme can compensate for the bandwidth limitation of a linear transmission channel with relaxed requirements on driver linearity. By trading-off the optical extinction ratio of the transmitted signal, we show that the optical EQ can provide a more open eye that yields significant improvement in receiver sensitivity and jitter compared to no equalization [6]. In this section, we experimentally investigate the use of optical EQ on a segmented MZM variant with 400  $\mu$ m segment length at 25 Gb/s NRZ transmission.

### A. Experimental Setup

Fig. 5 depicts the diagram of the high-speed experimental setup. A multi-channel pattern generator is employed to generate synchronous pseudo-random binary sequences (PRBSs) to provide driving signals to 6 channels of the driver IC. Electrical phase shifters are used to finely control the delay of the driving signals. In reality, input signal distribution can be implemented by a resistor network and buffers for delay control. The RF input signals were routed through SMP connectors on the PCB across micro-strip transmission lines and terminated into the on-chip 50  $\Omega$  terminations. The differential output of each channel of the IC drives each segment of the modulator in push-pull configuration. DC biases are provided to the PCB through ribbon cables. As described above, the driver IC would require two level DC voltages:  $V_{\rm DD1}$  is biased at 1 V and  $V_{\rm DD2}$  is biased at 2 V. A

source-meter is employed to bias the cathode of the modulator at 3 V which provides optimum extinction ratio of modulated optical signal. A dual channel DC power supply is used to bias the two heaters in order to set the MZM at its quadrature point.

A commercial telecom-grade distributed feedback (DFB) laser is used to provide input light at a wavelength of 1314 nm. The power consumption of the laser is 205 mW (not including the power consumption of the temperature controller). A polarization controller is placed before the modulator to optimize the polarization of light launched into the modulator. The light is edge-coupled to the silicon modulator through single-mode tapered-lensed fibers positioned with 3-axis precision stages. The inset of Fig. 5 shows the output optical spectrum from the modulator. Output light from the modulator is tapped 1% for power monitoring, while 99% passes through an optical amplifier (OA). Finally, an optical switch was used to select between a sampling scope with a 30-GHz photo-detector plugin, an optical average power meter, or a reference receiver (Rx), which is a commercial 43 Gb/s receiver with integrated trans-impedance amplifier (TIA) and limiting amplifier. The differential electrical output signal from the receiver is then fed into the BER tester and the sampling scope. A signal generator is deployed to provide the external clock for the pattern generator, the BER tester and the scope trigger. Receiver sensitivity measurements are presented by plotting BER versus optical modulation amplitude (OMA). The OMA axis is calibrated by the received power measured from the optical average power meter and the extinction ratio at low bitrate (5 Gb/s). The timing margin of the NRZ signal is measured by taking bathtub curves at high OMA and extracting the jitter values from well-known jitter models. To perform optical EQ, the main tap segments are driven by the same pattern with matched delay while the EQ tap segments are driven with an inverted pattern and optimized delay. The optical coupling loss is  $\sim$ 3 dB per facet, and at the quadrature point, the total insertion loss of the MZM is 6 dB.

#### B. Results and Discussion

We run the transmission experiment at 25 Gb/s and explore both 2-tap and 3-tap EQ implementations. The transmitter is first operated without EQ (i.e. 1 tap), then optical EQ with 2 taps and 3 taps is tested using PRBS-7 pattern. Fig. 6 shows the optical eye diagrams. The optical eyes consistently show the decreasing in amount of inter-symbol interference (ISI) when larger degrees of equalization are applied. However, the extinction ratio of the NRZ signal is reduced with more taps. The measured extinction ratio is 7.1 dB without optical EQ, 4.9 dB with 2-tap EQ, and to 2.4 dB with 3 taps.

The improvement in timing margin with optical EQ is further investigated by measuring the bathtub curves with and without equalization using PRBS-15 sequence. Fig. 7 presents the jitter measurement results at -1.9 dBm received power. It can be seen that the optical EQ significantly improves the jitter of the link. At 25 Gb/s, without EQ, the bathtub curve at -1.9 dBm received power is closed showing an error floor at BER  $=10^{-6}$ . When turning on the EQ, jitter measurement shows an open bathtub curve yielding  $\sim$ 0.2UI eye-opening at BER  $=10^{-10}$ .

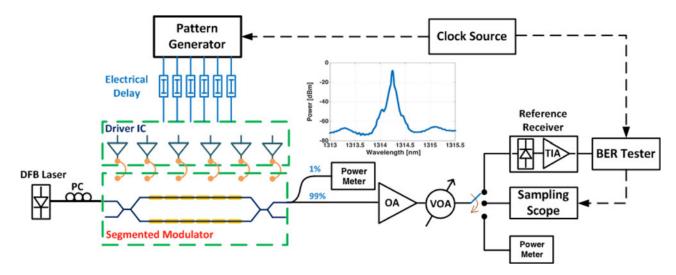


Fig. 5. Experiment setup for optical link with NRZ signaling.

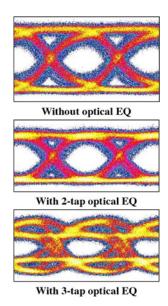


Fig. 6. Transmitted optical eye at 25 Gb/s for 400  $\mu$ m-segment MZM with PRBS-7 pattern.

Fig. 8 plots the receiver sensitivity measurement results with 400  $\mu$ m-segment modulator at 25 Gb/s bitrate with and without equalization. The BER versus OMA curves in Fig. 8 confirm the significant improvement in receiver sensitivity when using optical equalization. Without EQ, an error floor appears at  $BER = 10^{-11}$  while with EQ, error free back-to-back transmission can be achieved with BER  $= 10^{-12}$  at -4 dBm OMA with 2-tap EQ and -8 dBm with 3-tap EQ. As discussed above, higher degrees of equalization yield more improvement in receiver sensitivity but with lower extinction ratio. An optimum operation point with 3-tap EQ has been found in this particular transmitter. As shown in Fig. 8, a 4 dB penalty at BER =  $10^{-12}$ is observed when reducing the number of EQ taps from 2 to 1. The power consumption of the transmitter subsystem is 143 mW including 140.6 mW from the CMOS driver IC (not including power dissipated on 50  $\Omega$  input termination) and 2.4 mW

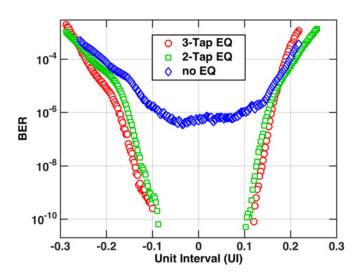


Fig. 7. Optical equalization enlarges the time margin in the bathtub curves at 25 Gb/s for 400  $\mu m$ -segment MZM.

from the heaters. This yields a power efficiency of 5.7 pJ/bit at 25 Gb/s operating bitrate. The results consolidate the advantage of low driver power consumption in CMOS technology. As a point of reference, a state-of-the-art BiCMOS driver for a silicon photonic transmitter has been reported with 450 mW power consumption [15].

# IV. PAM-4 SIGNALING WITH SEGMENTED MODULATOR

Recently, PAM-4 signaling has been considered as the modulation format for the next 400G Ethernet standard [16]. Extensive research and development has been published to investigate the performance as well as the feasibility of this high order modulation format for commercial deployments [17], [18]. In this section, we show that our flexible transmitter can also be used to transmit PAM-4 signal. To generate an optical PAM-4 signal with a segmented modulator and multi-channel driver IC, only a small change in driving condition is involved.

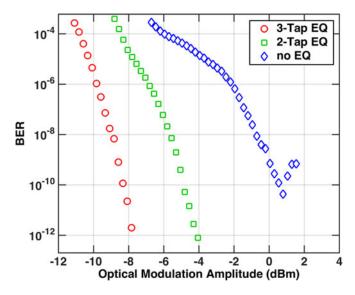


Fig. 8. Equalization improves the receiver sensitivity for optical link operating at 25 Gb/s with 400  $\mu m$ -segment MZM.

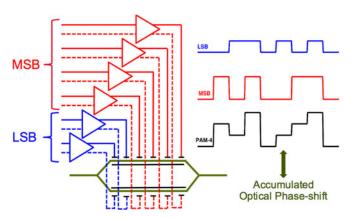


Fig. 9. PAM-4 signal generation with segmented MZM and multi-channel driver IC.

As illustrated in Fig. 9, the 4-level PAM signal can be simply generated with multi-equal-segment MZM by driving N segments with the least-significant-bit (LSB) stream and 2  $\times$  N segments with the most-significant-bit (MSB) stream. In this section, we report the experimental results of PAM-4 signaling with a 300  $\mu$ m-segment MZM without and with advanced signal processing up to 46Gb/s.

# A. PAM-4 Signal Transmission Experiments

The experimental setup for PAM-4 signaling is similar to the setup for NRZ described in the previous section except for some small changes as follow. The first 2 segments of the MZM are driven by the same pattern from the LSB stream while the MSB stream drives the remaining 4 segments of the device. The MSB is derived from PRBS-7 sequence and the LSB is from the same PRBS-7 sequence with 10-bit delay to de-correlate the two bit streams forming a PAM-4 symbol sequence. All six driving signals are tuned to match the phase delay as with NRZ signaling. At the receiver side, the reference limiting receiver

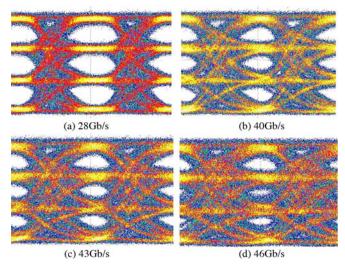


Fig. 10. Transmitted optical eye at different bitrate from the 300  $\mu \mathrm{m}\text{-segment}$  MZM.

for NRZ signal was replaced by a reference linear receiver with 20 GHz bandwidth. Instead of directly measuring real-time BER by a BER tester (BERT) as with NRZ signaling, the electrical signal output from the receiver is captured at 80Gsamples/s oversampling rate by a real-time scope with 32 GHz bandwidth. The captured signal is then used for offline BER estimation.

Fig. 10 shows the optical eyes at different bitrate recorded by the sampling scope with a 30 GHz bandwidth optical plugin. The optical eyes demonstrate even-spacing between the four levels of the signal which would suggest that the modulator was well driven in the linear region around the quadrature point of the MZM transfer function. The measured extinction ratio (between level-0 and level-3 of PAM-4 signal) for 28 Gb/s in Fig. 10(a) was 2.8 dB. At high bitrate, significant ISI degraded the vertical eye opening, especially the middle-level eye, as in Fig. 10(d). The extinction ratio of the transmitted signal could be improved by modifying the MZM design as follows: (1) increasing the length of each segment with the trade-off of increasing the segment capacitance, (2) increasing the number of segments with accompanying increase in the number of drivers and power consumption.

# B. BER Performance of PAM-4 Signaling

To measure the BER performance of the PAM-4 transmitter, the captured signal from the real-time scope is fed into a computer and processed with MATLAB for basic blocks in the receiver. The signal is first resampled and the clock recovery is performed to find the sampling phase. The signal is then down-sampled to one sample per symbol to reconstruct the received symbols. The symbol stream is subsequently demodulated into bit streams and directly compared with the transmitted bit streams for BER estimation. Initially, no advanced digital signal processing (DSP) is applied to the received signal. More than 1Mbit was used in BER estimation for each data point in the BER curves. That would yield a good estimation down to BER  $\sim 10^{-5}$ . A minimum mean squared error (MMSE)

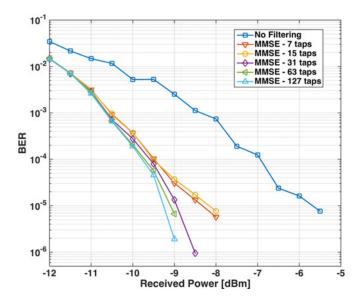


Fig. 11. BER performance at different MMSE tap-lengths for 40 Gb/s PAM-4 signaling with 300  $\mu \text{m}$ -segment MZM.

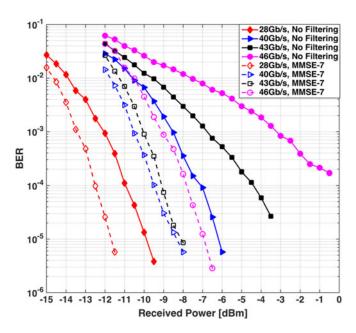


Fig. 12. BER performance of PAM-4 signaling with and without 7–tap MMSE equalizer at different bitrate for 300  $\mu$ m-segment MZM.

equalization filter could be added to the signal processing to improve BER performance with a trade-off of DSP complexity required for receiver implementation.

Fig. 11 shows the BER performance versus received optical power for 40 Gb/s PAM-4 signal without and with MMSE equalization (filtering). Even without advanced DSP, the 40 Gb/s PAM-4 signal demonstrated good BER performance, operating well below hard-decision pre-FEC (7% overhead) limit (BER =  $3.8 \times 10^{-3}$ ). The MMSE equalizer would improve receiver sensitivity about 2 dB at BER =  $10^{-3}$ . When increasing the tap-length (2N-1) of the MMSE equalizer from 7-taps to 127-taps, the BER is slightly improved. That would

suggest the 7-tap length MMSE equalizer is sufficient for this transmission link.

Fig. 12 plots the BER performance of PAM-4 signaling at different bitrates. At 46 Gb/s, without advanced DSP, BER below the pre-FEC limit is achieved, but would require high received power, -3 dBm for BER  $= 10^{-3}$ . The 7-tap MMSE equalizer significantly improves receiver sensitivity by 6 dB at BER  $= 10^{-3}$  with larger BER-curve slope at this data rate. A 5.5 dB penalty at BER  $= 10^{-3}$  could be observed when moving from 40 Gb/s to 46 Gb/s without DSP and is reduced to 1.5 dB penalty with 7-tap MMSE equalization. Obviously, at low bitrate when operating well below the bandwidth limitation of the system, the benefit provided by the digital equalizer would be less (eg. 1.5 dB penalty at 28 Gb/s). At 46 Gb/s PAM-4, the transmitter subsystem power consumption is 130.5 mW corresponding to a power efficiency of 2.8 pJ/bit.

#### V. CONCLUSION

In this paper, we demonstrated a flexible silicon photonics transmitter using a segmented MZM. The silicon modulator was driven by a 6-channel 32 nm CMOS driver IC wire-bonded in the same package. Error free transmission at 25 Gb/s NRZ is achieved with optical EQ. The transmitter further provides flexibility in varying the EQ's tap weight by altering the ratio of segments devoted to main and equalizing signals. PAM-4 signal transmission at 46 Gb/s with BER well below pre-FEC limit is also reported. The transmitter presents the ability to effectively perform adaptive PAM modulation formats by simply manipulating the segment-driving scheme while exhibiting very low power consumption. The energy efficiency of the driver IC could be further improved in the future design where the channels for the same bit stream would share some common amplifier stages. That shows the potential of a flexible silicon photonics transmitter for fast-reconfigurable agile optical networks.

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