Four-Channel WDM Transmitter With Heterogeneously Integrated III-V/Si Photonics and Low Power 32 nm CMOS Drivers

Tam N. Huynh, Anand Ramaswamy, Renato Rimolo-Donadio, *Member, IEEE*, Clint Schow, *Senior Member, IEEE, Senior Member, OSA*, Jonathan E. Roth, Erik J. Norberg, Jonathan Proesel, *Member, IEEE*, Robert S. Guzzon, Jaehyuk Shin, Alexander Rylyakov, *Senior Member, IEEE*, Christian Baks, Brian Koch, Daniel Sparacin, *Member, IEEE*, Greg Fish, *Senior Member, IEEE*, and Benjamin G. Lee, *Senior Member, IEEE, Senior Member, OSA*

***Abstract*—We experimentally demonstrate a novel four-channel wavelength division multiplexing transmitter operating at $1.3\ \mu$m wavelength employing heterogeneously integrated III-V/Si photonic circuit copackaged with low-power 32-nm SOI CMOS driver integrated circuits (ICs). Error-free operation ($\mathrm{BER} < 10^{-12}$) has been achieved across all four channels for back-to-back, 2 and 10 km single-mode fiber transmission at 25 Gb/s per each channel, targeting intra- and inter-datacenter interconnect applications. Power consumption as low as 19.2 mW for four CMOS driver ICs has been recorded, which yields 0.19 pJ/bit energy efficiency.**

***Index Terms*—CMOS integrated circuits (ICs), silicon photonics, tunable lasers, wavelength division multiplexing (WDM) transmitter.**

I. Introduction

RECENTLY datacenter interconnects have witnessed ever-increasing growth in the bandwidth requirement which is driven by bandwidth-intense applications such as social media networks, online streaming, and cloud computing. To address this exponential growth in data traffic, high bandwidth, energy efficient and low cost optical transceivers are needed. While today the short-reach optical interconnects (<100 m) inside the datacenter are dominated by low cost multimode VCSEL-links, there is a growing demand for longer reach optical links in intra and inter-datacenter interconnects (up to 10 km) for datacenter expansion. Single-mode fiber (SMF) optical links employing silicon and/or heterogeneous III-V/Si photonics manifest themselves as promising candidates for this market due to their potential for realizing an integrated wavelength division multiplexing (WDM) transceiver with low cost [1]–[10]. Integration technologies varying from monolithic silicon photonics [1]–[4] to hybrid III-V/Si [5]–[10] have been investigated extensively in academia as well as industry. The monolithic integration solution would enable low component parasitics, simplify packaging with the tradeoff in tuning fabrication process for best electronic or photonic device performance [9]. In contrast the heterogeneous integration approach would benefit from the independent platforms for electronic and photonics integrated circuits (ICs) to optimize performance for each part of the system with the disadvantages in parasitics due to packaging. This issue could be mitigated by short wire bonds or flip-chip bonding and co-design, co-package between electronic and photonic parts [8]–[10]. Moreover reaching the aggressive bandwidth targets outlined in next generation standards, such as 400 Gb/s Ethernet [11], requires significant improvements over current commercial technologies, and is more easily achieved when scaling both data rate and channel count. Here, we investigate the potential of high-channel-count transmitters by assembling and characterizing a densely integrated photonic circuit with low-power CMOS drivers. The density and efficiency afforded by advanced CMOS electronics and heterogeneously integrated III-V/Si photonics provide promise for scaling channel counts in the future while maintaining aggressive cost and power targets.

Previously, four-channel silicon photonic transmitters have been reported up to 27 Gb/s per channel [3]–[6]. A $4\lambda \times 12.5\,\mathrm{Gb/s}$ WDM silicon photonics link was reported in [5] followed by a demonstrating of 25 Gb/s single channel transmission [6] based on the same technology platform. Hybrid III-V/Si integration had been introduced to fabricate DBR lasers for transmitter. In [3] an integrated $4 \times 25\,\mathrm{Gb/s}$ parallel optical transceiver had been fabricated on monolithic silicon photonics platform leveraging the 130 nm CMOS SOI process. The transmitter employed Mach-Zehnder modulators based on p-i-n junction and a hermetic micro-packed DFB laser as an off-chip

Manuscript received March 28, 2016; revised May 27, 2016; accepted June 06, 2016. Date of publication June 09, 2016; date of current version June 22, 2016. This work was supported in part by the Defense Advanced Research Projects Agency and by the Army Research Laboratory under Contract W911NF-12-2-0051.

T. N. Huynh, J. Proesel, C. Baks, and B. G. Lee are with the IBM T. J. Watson Research Center, New York, NY 10598 USA (e-mail: tnhuynh@us.ibm.com; jonproesel@us.ibm.com).

A. Ramaswamy, J. E. Roth, E. J. Norberg, R. S. Guzzon, J. Shin, B. Koch, D. Sparacin, and G. Fish are with the Aurrion, Inc., Goleta, CA 93117 USA (e-mail: anand.ramaswamy@aurrion.com; jon.roth@aurrion.com; erik.norberg@aurrion.com; rob.guzzon@aurrion.com; jaehyuk.shin@aurrion.com; Brian.Koch@aurrion.com; daniel.sparacin@aurrion.com; greg.fish@aurrion.com).

R. Rimolo-Donadio was with the IBM T. J. Watson Research Center, New York, NY 10598 USA. He is now with the Costa Rica Institute of Technology, Cartago 30101, Costa Rica (e-mail: rrimolo@itcr.ac.cr).

A. Rylyakov was with the IBM T. J. Watson Research Center, New York, NY 10598 USA. He is now with the Coriant Advanced Technology Group, New York, NY 10016 USA (e-mail: Alexander.Rylyakov@coriant.com).

C. Schow was with the IBM T. J. Watson Research Center, New York, NY 10598, USA. He is now with the University of California at Santa Barbara, Santa Barbara, CA 93106 USA (e-mail: schow@ece.ucsb.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JLT.2016.2578644

continuous-wave light source. While the $4 \times 25\,\mathrm{Gb/s}$ parallel transmitter in [4] included the Ge-Si transverse PIN structure electro-absorption modulators (EAMs). In our previous work reported in [8], we had demonstrated a four-channel silicon photonics WDM transmitter with integrated lasers and EAMs driven by 32 nm CMOS driver ICs operating error-free (BER $<10^{-12}$) at 4×28 Gb/s over 10 km SMF fiber. The key element that enables good performance with such extremely low power consumption in our (current and previously reported) driver circuits is the shift from remote drivers interfaced with the photonic integrated circuit (PIC) through $50\,\Omega$ transmission lines requiring impedance matching to tightly co-packaged electronics and photonics.

In this paper, we report the experimental measurements of a four-channel WDM transmitter with similar PIC but driven by a modified 32 nm CMOS driver IC. The difference in the IC design is targeting lower power consumption by reducing the output stage voltage from $2\,\mathrm{V_{pp}}$ [8, 10] to $1\,\mathrm{V_{pp}}$ while maintaining acceptable optical extinction ratio. The new IC design could achieve extremely low power consumption of 19.2 mW for driving four channels simultaneously while the lasers consume $\sim$1.1 W and the EAMs consume 28.5 mW. The state-of-the-art commercially available four-channel 25/28 Gb/s EAM driver IC with variable output swing (1.0–2.5 $\mathrm{V_{pp}}$) and other bias, control circuits has power consumption of 0.75 W per channel at 2.5 Vpp output [12]. The organization of the paper is as follow: Section II discusses the design of the PIC and the driver ICs employed in the four-channel WDM transmitter, Section III reports the experimental measurements and results, and finally, Section IV concludes the paper.

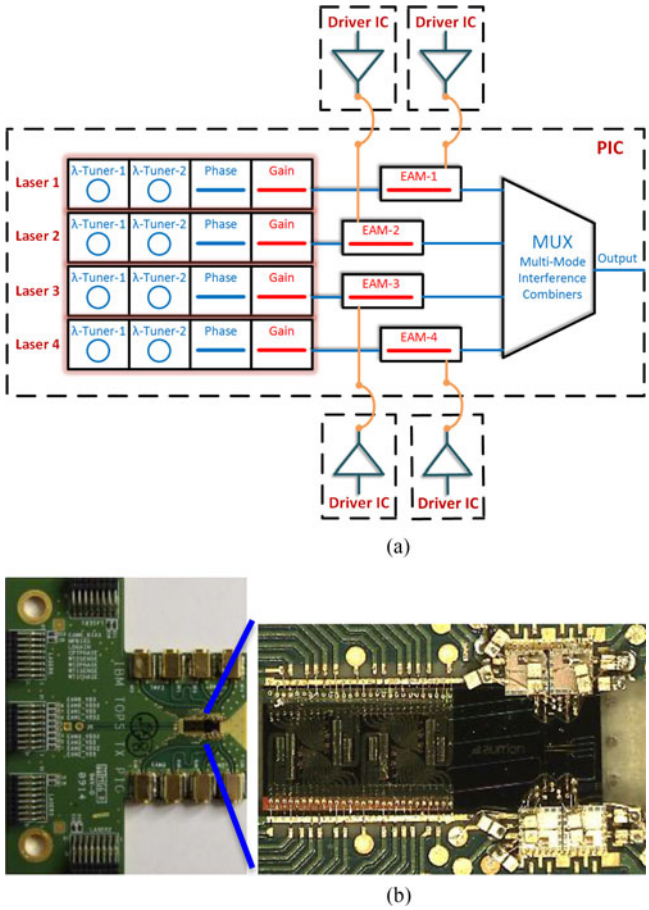

Fig. 1. (a) Conceptual design of the heterogeneously integrated four-channel WDM transmitter and (b) the custom PCB with micrograph of the transmitter.

II. PIC and Driver ICs Design

Fig. 1(a) illustrates the conceptual block diagram of the four-channel WDM transmitter, which consists of the heterogeneously integrated PIC co-packaged with the 32 nm SOI CMOS driver ICs. The photonic device was fabricated using III-V material heterogeneously integrated with silicon waveguides in an established foundry infrastructure with Aurrion's heterogeneous integration process. The four individual driver ICs were wire-bonded to the four EAMs. The PIC and driver ICs were co-packaged on a custom printed circuit board (PCB) for experimental measurements. Fig. 1(b) shows the image of the custom PCB together with the micrograph of the packaged four-channel WDM transmitter. The decoupling capacitors have been deployed to decouple noise from DC power supplies to the ICs. In the subsequent sections, we present details of the PIC and the driver IC.

A. Heterogeneous Integrated III-V/Si PIC

As illustrated in Fig. 1(a), the PIC demonstrated in this work consists of four tunable lasers [8], which are individually coupled to four EAMs. The fundamental design of the tunable lasers is similar to other well-known III-V material multisection tunable lasers [13]. The tunable laser in this design constitutes a gain section with two wavelength tuners and a phase tuning section. The lasers demonstrate side mode suppression ratios exceeding 40 dB with about 1 W power consumption for all four lasers. The gain section of the lasers was formed by heterogeneously bonding InP onto the silicon waveguide. Similar to the laser gain sections, the EAMs were fabricated simultaneously using Aurrion's heterogeneous integration process. The detailed characterization of the EAMs had been reported in [9] and [10]. The EAMs provide wide bandwidth ($\sim$30 nm) with low insertion loss ($<$3 dB) and low drive voltage (1–2 V_{pp}). Characterization of the wavelength tunability of the individual tunable laser in the transmitter was carried out by biasing the gain section at 150 mA, stabilizing the temperature of the entire WDM transmitter at 32 °C and performing wavelength tuning on the two wavelength tuner sections. Finally the modulated optical signals output from the EAMs will be multiplexed in the multimode interference (MMI) combiners. The MMI multiplexer experiences high insertion loss ($\sim$6 dB) when combining all four channels, but is employed due to its broad bandwidth to reduce risk in this prototype demonstration. The entire four-channel transmitter PIC occupies $2.75\,\mathrm{mm} \times 7.6\,\mathrm{mm}$.

B. 32 nm CMOS Driver ICs

The driver ICs were fabricated in IBM's standard 32 nm SOI CMOS technology (now Global Foundries) using standard thin

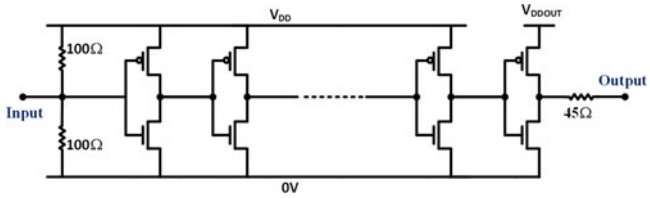

Fig. 2. Circuit design of the single channel $1\,V_{\rm pp}$ 32 nm SOI CMOS driver integrated circuit.

oxide transistors. Each single channel driver IC has a simple architecture as depicted in Fig. 2, targeting lower power consumption. $V_{\rm DD}$ is dc biased at 1V. The single-ended RF input signal is received into the on-chip $50\,\Omega$ termination. This $50\,\Omega$ termination at the driver IC input is added for impedance matc hing with standard $50\,\Omega$ characteristic impedance of laboratory equipment (particularly the output from the bit pattern generator in this work). Subsequently, the signal propagates through 6 consecutive CMOS inverters with increasing transistor gate-size to provide signal amplification up to full-swing CMOS level ($1\,V_{\rm pp}$). The amplified signal then drives the output stage, which is a CMOS inverter with a separate $V_{\rm DDOUT}$ supply followed by a series on-chip $45\,\Omega$ resistor. This resistor is employed for damping the ringing potentially caused by the wire-bond inductance and the EAM capacitance. Finally the driver output was wire-bonded to the anode of the EAM, while significant decoupling is applied to the EAM cathode supply. The pad-limited area of each single channel driver IC is $1\,{\rm mm} \times 1\,{\rm mm}$, while the core circuits occupy $18\,\mu{\rm m} \times 70\,\mu{\rm m}$.

Before bonding to the laser-integrated PIC, a 4-channel variant of the driver IC is characterized by wire-bonding to a 4-channel EAM photonic chip [10] and assembling on a PCB as in Fig. 3(a) for evaluating the multichannel performance of the electro-optic interface. A commercial DFB laser emitting at wavelength of 1310 nm with optical output power of 13 dBm was employed to couple light into the EAM chip. The fiber-coupled output power from the EAM was ∼–8 dBm. An O-band optical amplifier had been used to compensate for the coupling loss. The test was running with PRBS-31 sequence. The optical eyes were captured by a 30-GHz Tektronix scope plugin module and depicted in Fig. 3(b–f).

At target bitrate (25 Gb/s), the optical eye in Fig. 3(c) was well opened with low jitter. That would suggest a good driving signal condition for the integrated transceiver at $4 \times 25\,{\rm Gb/s}$. The optical extinction ratio at 20 Gb/s as in Fig. 3(b) was 5.2 dB when biasing the EAM at 2.5 V. The biasing of the EAMs was adjusted to optimize the optical extinction ratio that would yield a lower crossing point in the observed optical eyes. Further characterization results in Fig. 3 demonstrate that the $1\,V_{\rm pp}$ driver IC could yield an open optical eye up to 35 Gb/s with relatively low jitter. The measured optical eyes at bitrate above 25 Gb/s indicate an increasing inter-symbol interference level that leads to a higher vertical eye closure penalty at higher data rate. This bandwidth limitation is attributed for the bandwidth limit of the driver ICs based on 32 nm CMOS technology which would be lower the bandwidth of the EAMs.

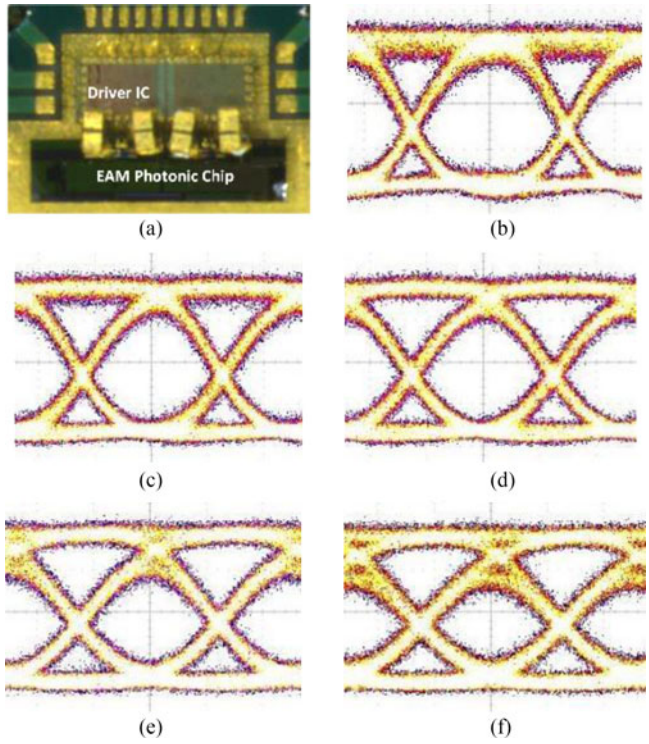

Fig. 3. (a) Testing assembly of the driver IC, and (b–f) optical eyes at different bitrates from 20 to 35 Gb/s.

III. Experiments and Results

In this section we describe the experimental demonstration and the measurement results of the heterogeneously integrated four-channel WDM transmitter. The experiment setup to measure the bit error rate (BER) performance of all four channels of the transmitter will be first presented, following by the discussion on the measured BER results.

A. Experiment Setup

The experiment setup is illustrated in Fig. 4(a). As presented in the previous section, the PIC and driver ICs were wire-bond co-packaged on a custom PCB. The four single-ended RF input signals were routed through MMPX connectors at the card edge across micro-strip transmission lines and terminated into the on-chip $50\,\Omega$ terminations. The PCB has cutouts for edge-coupled access using single-mode tapered-lensed fibers positioned with 3-axis precision stages. DC biases for driver ICs and PIC were provided through ribbon cables. $V_{\rm DD}$ of the driver ICs was biased at 1 V. A 12-channel current source was employed to bias the gain section and two wavelength tuners (heaters) for all four lasers. In addition, two dual-output low noise Agilent sources were used for fine-tuning the phase sections of the lasers (when needed). The operating wavelength of four lasers had been tuned to match with 100GBASE-LR4 grid. Table I presents the bias parameters for the lasers (no phase tuning was needed in this operating condition) and the measured wavelength of the four lasers. Fig. 4(b) illustrated the optical spectrum of the four channels being used. The whole WDM transmitter was

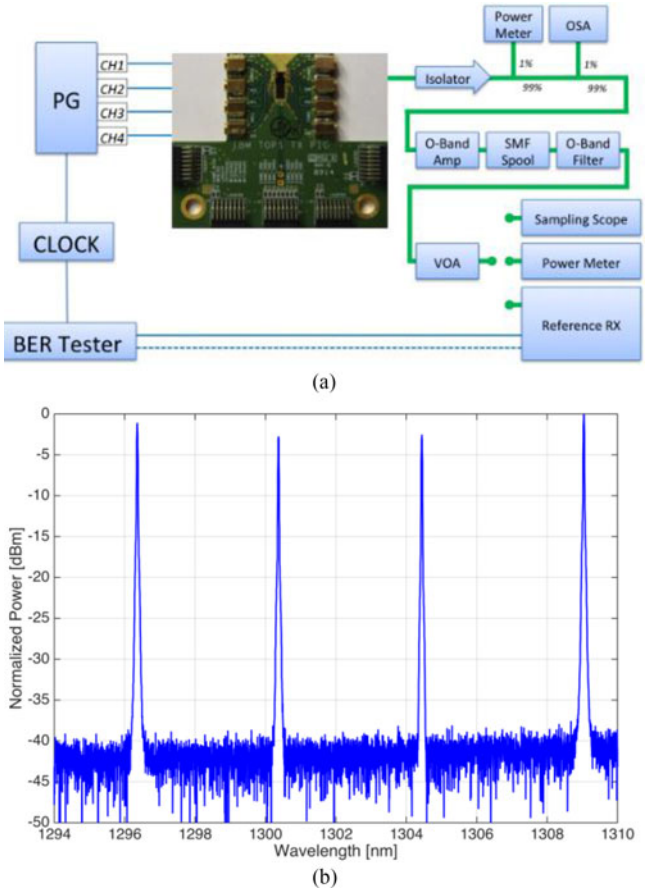

Fig. 4. (a) Experiment setup for BER measurement of the four-channel WDM transmitter and (b) measured optical spectrum of the multiplexed four channels at the transmitter output.

TABLE I
OPERATING CONDITION OF WDM TRANSMITTER

Parameters	Channel 1	Channel 2	Channel 3	Channel 4
Wavelength	1296.3 nm	1300.3 nm	1304.4 nm	1309 nm
Gain Current	149.75 mA	149.74 mA	149.61 mA	149.43 mA
λ-Tuner-1	14.70 mA	12.95 mA	1.23 mA	0.97 mA
λ-Tuner-2	28.98 mA	24.89 mA	23.96 mA	22.14 mA
EAM Bias	2.30 V	2.40 V	2.90 V	3.30 V
Extinction Ratio	3.49 dB	3.27 dB	3.68 dB	3.87 dB

temperature stabilized at 32 °C by a thermal electric-cooler (TEC).

Four source-meters were employed to independently bias four EAMs. Table I shows the biasing voltage for each EAM, ranging from 2.3 to 3.3 V. That yields the extinction ratio of the modulated optical NRZ signals from 3.3 to 3.9 dB as shown in the same table. Two super high frequency (SHF) BPG-40A pattern generators were used to simultaneously provide four decorrelated 700 mV peak-to-peak RF signals input to the four single-channel driver ICs. The pattern generators were operating at 25 Gb/s with an external clock source. All the BER measurements were running with PRBS-31 sequence.

Light was extracted from the PIC using a single-mode tapered-lensed fiber with an approximate $2.5\,\mu\mathrm{m}$ spot diameter.

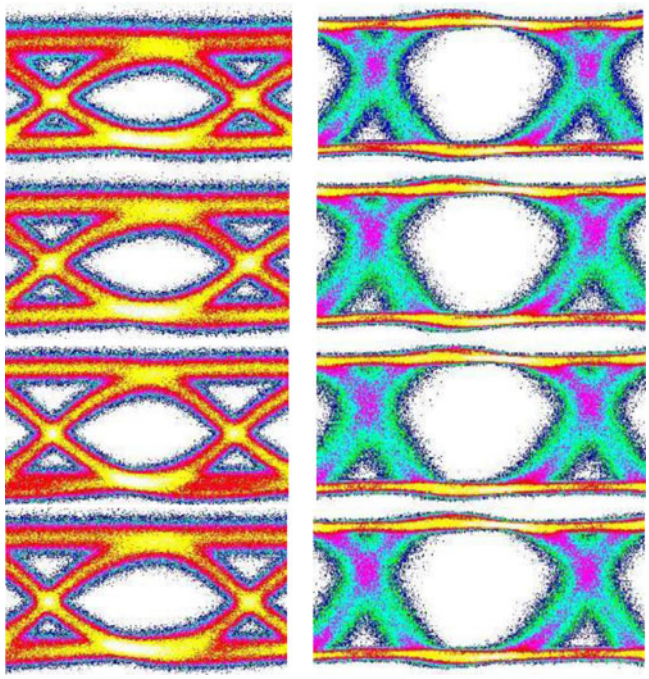

Fig. 5. Transmitted optical eyes (left) and received electrical eyes (right) for all four channels (channel 1 to 4 from top to bottom) at 25 Gbit/s, back-to-back link.

The light was then passed through an isolator, a praseodymium-doped fiber amplifier, a spool of SMF (10 km or 2 km), a tunable Fabry–Perot filter, and a variable optical attenuator. Optical amplification is required to compensate for coupling loss. Finally, an optical switch was used to select between a sampling scope with a 30-GHz photo-detector plugin, an optical average power meter, or a reference receiver (Rx). The Rx consists of a custom 130-nm SiGe IC, similar to the receiver used in [14] but with a DC-coupled transimpedance stage, wire-bonded to a commercial photo-detector with 0.6 A/W responsivity at 1310 nm. The RX's differential outputs were connected to an SHF error detector. The transmitter was tested with all channels running simultaneously, filtering out one channel at a time on the Rx.

B. Measurement Results

Fig. 5 shows the transmitted optical and received electrical eyes at 25 Gb/s per channel of all four channels of the WDM transmitter. The optical eye is open across all channels with the extinction ratio ranging from 3.3 to 3.9 dB. That is about 3 dB lower than the extinction ratio of the WDM transmitter driven by $2\,V_{\mathrm{pp}}$ output driver ICs in [8]. It's worthwhile to note that for targeting lower driver IC power consumption by deploying $1\,V_{\mathrm{pp}}$ output stage driver ICs, we have to trade-off the optical extinction ratio as well as the operating bitrate of the optical link. The estimated signal-to-noise ratio from the captured eye diagrams suggest that error-free transmission would be achieved across all channels.

The BER measurement results are presented in Fig. 6 confirming the error-free operation for all four channels at targeted bitrate 25 Gb/s per each channel. The BER curves were recorded for each channel at 25 Gb/s for back-to-back, 2 and 10 km SMF

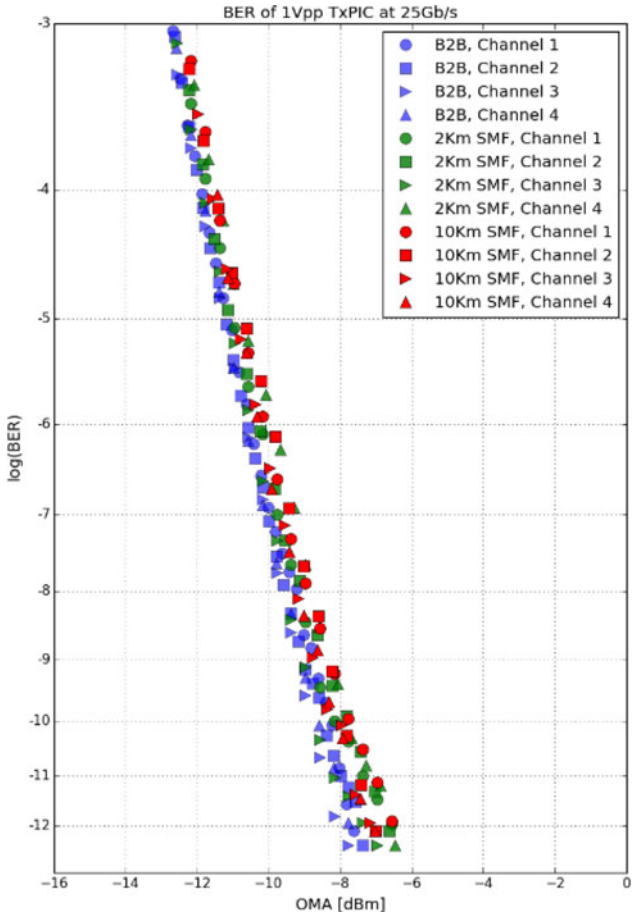

Fig. 6. BER measurements of the heterogeneously integrated four-channel WDM transmitter at 25 Gb/s per each channel over back-to-back, 2 and 10 km SMF fiber transmission link.

TABLE II
POWER CONSUMPTION OF WDM TRANSMITTER

Part	Power Consumption [mW]	Energy Efficiency [pJ/bit]
Lasers	1103.85	11.04
EAMs	28.54	0.29
Driver IC	19.2	0.19
Total	**1151.6**	**11.5**

transmission. The BER curves are plotted against the measured optical modulation amplitude. The curves for four channels exhibit a spread of about 1 dB at $\mathrm{BER} = 10^{-12}$, attributed to the variation in package parasitic. A negligible penalty, less than 1 dB at $\mathrm{BER} = 10^{-12}$, is observed between back-to-back and fiber transmission (2 and 10 km SMF). This penalty could be attributed to the small fiber dispersion as well as the temperature variation along the transmission fiber and the lack of clock & data recovery block at the receiver to correct for these small fluctuations. The transmission measurement results demonstrate the feasibility of the designed WDM transmitter for intra and inter data center interconnect applications.

Table II shows the break down of power consumption of the heterogeneously integrated WDM transmitter operating at aggregated bitrate of 100 Gb/s. The driver ICs (four single-channel 32 nm CMOS ICs) consume 19.2 mW in total, not counting the DC current caused by the input termination, which yields an energy efficiency of 0.19 pJ/bit. In practice, the $50\,\Omega$ termination and its' power consumption is typically considered as part of the upstream component and not accounted for EAM driver circuit. As targeting in the IC design, the power consumption of the $1V_{\mathrm{pp}}$ driver ICs is significantly lower than that of the $2V_{\mathrm{pp}}$ driver ICs: 97.6 mW at 4×28 Gb/s or 0.87 pJ/bit energy efficiency [8]. The EAMs consume 28.54 mW while the lasers consume 1.1 W. That leads to the total power consumption of the WDM transmitter of 1151.6 mW at 100 Gb/s operation yielding an energy efficiency of 11.5 pJ/bit. (The calculation above does not include the additional power consumption of the TEC.)

IV. CONCLUSION

We have demonstrated a four-channel WDM transmitter employing heterogeneously integrated III-V/Si photonic circuits and 32 nm SOI CMOS driver ICs. The transmitter achieved error-free transmission over 10 km SMF at 25 Gb/s per channel. A power efficiency of 11.5 pJ/bit for the transmitter including lasers, modulators and driver ICs had been recorded. The driver ICs themselves consume only 19.2 mW correspondingly 0.19 pJ/bit energy efficiency.

The measurement results show the feasibility of the integrated WDM transmitter for intra and inter-data centers interconnect applications. This illustrates the potential of delivering on low power, low cost, high-channel-count WDM transceivers based-on hybrid III-V/Si photonic circuits and CMOS ICs technologies.

ACKNOWLEDGMENT

The views, opinions, and/or findings contained in this article are those of the authors and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government. Approved for Public Release, Distribution Unlimited.

REFERENCES

[1] S. Assefa *et al.*, "A 90 nm CMOS integrated nano-photonics technology for 25Gbps WDM optical communications applications," in *Proc. IEEE Int. Electron Devices Meet.*, 2012, pp. 33.8.1–33.8.3.
[2] D. M. Gill *et al.*, "Demonstration of a high extinction ratio monolithic CMOS integrated nanophotnic transmitter and 16 Gb/s optical link," *IEEE J. Sel. Topics Quantum Electron.*, vol. 21, no. 4, 2015, Art. no. 3400311.
[3] T. Pinguet *et al.*, "25 Gb/s silicon photonic transceivers," in *Proc. IEEE Int. Conf. Group IV Photon.*, 2012, pp. 189–191.
[4] S. Jatar *et al.*, "Performance of parallel 4×25 Gbs transmitter and receiver fabricated on SOI platform," in *Proc. IEEE Int. Conf. Group IV Photon.*, 2012, pp. 159–161.
[5] B. Koch *et al.*, "A 4x12.5 Gb/s CWDM Si photonics link using integrated hybrid silicon lasers," presented at the CLEO Conf., Baltimore, MD, USA, 2011, paper CThP5.
[6] H. F. Liu, "Integrated silicon photonics links for high bandwidth data transportation," presented at the Optical Fiber Communications Conf. Exhibition, San Francisco, CA, USA, 2014, paper Th1D.1.
[7] M. L. Davenport *et al.*, "Hybrid silicon photonic integrated circuit technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 19, no. 4, 2013, Art. no. 6100117.
[8] A. Ramaswamy *et al.*, "A WDM 4x28Gbps integrated silicon photonic transmitter driven by 32 nm CMOS driver ICs," presented at the Optical

Fiber Communications Conf. Exhibition, Los Angeles, CA, USA, 2015, paper Th5B.5.
[9] N. Dupuis *et al.*, "30-Gb/s optical link combining heterogeneously integrated III–V/Si photonics with 32-nm CMOS circuits," *J. Lightw. Technol.*, vol. 33, pp. 657–662, 2015.
[10] B. G. Lee *et al.*, "A WDM-compatible 4×32-Gb/s CMOS-driven electroabsorption modulator array," presented at the Optical Fiber Communications Conf. Exhibition, Los Angeles, CA, USA, 2015, paper Tu3G.3.
[11] IEEE P802.3bs 400 Gb/s Ethernet Task Force, 2014. [Online]. Available: http://www.ieee802.org/3/bs/index.html.
[12] MACOM Product Detail: MAOM-02204A, 2014. [Online]. Available: http://www.macom.com/products/product-detail/MAOM-02204A.
[13] L. A. Coldren, "Monolithic tunable diode lasers," *IEEE J. Sel. Topics Quantum Electron.*, vol. 6, no. 6, pp. 988–999, Nov./Dec. 2000.
[14] A. V. Rylyakov *et al.*, "A 40-Gb/s, 850 nm, VCSEL-based full optical link," presented at the Optical Fiber Communications Conf. Exhibition, Los Angeles, CA, USA, 2012, paper OTh5E.1.

Tam N. Huynh was born in Dien Khanh, Khanh Hoa, Vietnam, in 1984. He received the B.S. degree from the Ho Chi Minh City University of Technology, Ho Chi Minh City, Vietnam, in 2007, and the M.Sc. and Ph.D. degrees from Dublin City University, Dublin, Ireland, in 2010 and 2014, all in telecommunication engineering. He is currently a Postdoctoral Researcher at the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA. His research interests include optical interconnects, semiconductor lasers, and coherent optical communications.

Anand Ramaswamy received the B.S. degree in electrical engineering with a minor in physics and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, CA, USA, and the University of California, Santa Barbara, Santa Barbara, CA, in 2005, 2007, and 2010, respectively. He is currently the Photonics Systems Manager at the Aurrion, Inc., Santa Barbara. His current research interests include photonic integrated circuits for optical communications. He holds 2 patents and has authored/coauthored more than 45 papers in the field of photonics.

Renato Rimolo-Donadio (S'08–M'11) received the B.S. and Lic. degrees in electrical engineering from the Technical University of Costa Rica (ITCR), Cartago, Costa Rica, in 1999 and 2004, respectively, the M.S. degree in microelectronics and microsystems, and the Ph.D. degree in electrical engineering, both from the Technical University of Hamburg-Harburg (TUHH), Hamburg, Germany, in 2006 and 2010, respectively. In 2014, he joined as a Professor at the Electronics Engineering Department, ITCR. From 2012 to 2014, he was with the IBM T.J. Watson Research Center, and from 2006 to 2012, with the Institute of Electromagnetic Theory, TUHH. His current research interests include system-level modeling and optimization of interconnects, analysis of signal and power integrity problems, and high-speed circuit design.

Clint Schow (SM'10) received the Ph.D. degree in electrical engineering from the University of Texas at Austin, Austin, TX, USA, in 1999. He joined IBM, Rochester, MN, USA, assuming responsibility for the optical receivers used in IBMs optical transceiver business. From 2001 to 2004, he was with the Agility Communications, Santa Barbara, CA, USA, developing high-speed optoelectronic modulators and tunable laser sources. In 2004, he joined the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, as a Research Staff Member and currently manages the Optical Link and System Design Group responsible for optics in future generations of servers and supercomputers. He has directed multiple DARPA-sponsored programs investigating chip-to-chip optical links, nanophotonic switches, and future systems utilizing photonic switching fabrics. He has published more than 150 journals and conference articles and has 16 issued patents. He is a senior member of the OSA.

Jonathan E. Roth was born in Lansdale, PA, USA, in 1977. He received the B.S. degree in biomedical engineering from Case Western Reserve University in Cleveland, OH, USA, in 2000, and the Ph.D. degree in electrical engineering from Stanford University in Stanford, CA, USA, in 2007. His dissertation work was on electroabsorption modulators in indium phosphide and silicon germanium. He is employed by Aurrion, Inc., as a Senior Optoelectronic Device Engineer, where he designs heterogeneous III–V on silicon devices and photonic integrated circuits.

Erik J. Norberg received the B.S. degree in engineering from Lund Technical University, Lund, Sweden, in 2008, and the Ph.D. degree in electrical engineering from the University of California, Santa Barbara (UCSB), Santa Barbara, CA, USA, in 2011. At UCSB, he developed integrated microwave photonic filters and demonstrated a high spur-free dynamic range integration platform on InP. He is currently a Senior Design Engineer at Aurrion, Inc., where he is developing integrated Si-photonic lasers and transceiver circuits. He is an author/coauthor of more than 45 papers in the field of photonics.

Jonathan Proesel (M'10) received the B.S. degree in computer engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 2004. He received the M.S. and Ph.D. degrees in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 2008 and 2010, respectively. He joined the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, in 2010, where he is currently a Research Staff Member working on analog and mixed-signal circuit design for optical transmitters and receivers. He has also held internships with IBM Microelectronics, Essex Junction, VT, USA, in 2004 and IBM Research, Yorktown Heights, in 2009. His research interests include high-speed optical and electrical communications, silicon photonics, and data converters. He is a member of the IEEE Solid-State Circuits Society. He received the Analog Devices Outstanding Student Designer Award in 2008, the SRC Techcon Best in Session Award for Analog Circuits in 2009, and co-received the Best Student Paper Award for the 2010 IEEE Custom Integrated Circuits Conference.

Robert S. Guzzon received the B.S. degree in electrical engineering and physics from Lehigh University in Bethlehem, PA, USA, in 2007, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Santa Barbara, CA, USA, in 2011, where his dissertation focused on the theory, design, and fabrication of high-SFDR photonic integrated microwave filter circuits. His current interests include the development of photonic integrated circuit systems and their electronic and optical interfaces.

Jaehyuk Shin received the B.S. degree in inorganic materials from Seoul National University, Seoul, Korea, in 1999, and the M.S. and Ph.D. degrees in materials science from the University of California, Santa Barbara, CA, USA, in 2007. He is currently the Design Automation Architect & Layout Manager at Aurrion, Inc., Santa Barbara. His current interests include development and integration of workflows for designing photonic integrated circuits.

Alexander Rylyakov (SM'15) received the M.S. degree from the Moscow Institute of Physics and Technology, Dolgoprudny, Russia, and the Ph.D. degree from the State University of New York (SUNY) at Stony Brook, Stony Brook, NY, USA, in 1989 and 1997, respectively, both in physics. From 1994 to 1999, he was with the Department of Physics, SUNY Stony Brook on integrated circuits based on Josephson junctions. From 1999 to 2014, he was a Research Staff Member with the IBM T.J. Watson Research Center, Yorktown Heights, NY, working on integrated circuits for wireline and optical communication, and on digital phase-locked loops. In 2015, he joined Coriant Advanced Technology Group as an Electronics Team Lead.

Christian Baks received the B.S. degree in applied physics from the Fontys College of Technology, Eindhoven, the Netherlands, in 2000, and the M.S. degree in physics from the State University of New York, Albany, NY, USA, in 2001. He joined the IBM T.J. Watson Research Center, Yorktown Heights, NY, as an Engineer in 2001, where he is involved in high-speed optoelectronic package and backplane interconnect design specializing in signal integrity issues.

Brian Koch received the Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara, CA, USA, in 2008. His dissertation was focused on optoelectronic resonators and mode locked lasers in photonic integrated circuits, with applications in optical clock recovery and optical signal regeneration. He was with the Intel's Photonics Technology Lab from 2008 to 2012, where he was involved in the designing and testing of heterogeneously integrated silicon lasers and other silicon-based photonic components and circuits. He is a Design Engineering Manager at Aurrion. Since joining Aurrion in 2012, he was with a design team developing novel devices and architectures on a silicon-based heterogeneous integration platform. He holds 6 patents and has authored more than 40 papers and 2 book chapters.

Daniel Sparacin received the B.S. degree in material science and engineering from Brown University, Providence, RI, USA, in 2000, and the Ph.D. degree from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2006, focused on silicon photonics device design and fabrication. After graduation, he was consulted for Defense Advanced Research Projects Agency Microsystems Technology Office in the areas of digital and RF photonic materials, devices, and systems. In 2012, he joined Aurrion, Goleta, CA, USA, where he is the Director of Technology.

Greg Fish (SM'11) received the B.S. degree in electrical engineering from the University of Wisconsin at Madison, Madison, WI, USA, in 1994, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 1999. He is the Chief Technology Officer at Aurrion, Goleta, CA, USA. He is considered as a Leading Expert in the field of photonic integration with nearly 20 years of experience in the field of InP-based photonic integrated circuits. He is an author/coauthor of more than 60 papers in the field and has 12 patents.

Benjamin G. Lee (M'04–SM'14) received the B.S. degree from Oklahoma State University, Stillwater, OK, USA, in 2004, and the M.S. and Ph.D. degrees from Columbia University, New York, NY, USA, in 2006 and 2009, respectively, all in electrical engineering. In 2009, he became a Postdoctoral Researcher at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, where he is currently a Research Staff Member. He is also an Assistant Adjunct Professor of electrical engineering at Columbia University. His research interests include silicon photonic devices, integrated optical switches and networks for high-performance computing systems and datacenters, and highly parallel multimode transceivers. He is a member of the Optical Society and the IEEE Photonics Society, where he served as an Associate Vice President of Membership. He serves on the technical program committees for the Optical Fiber Communications Conference and the Optical Interconnects Conference.